Datasheet

G32R502

Cortex®-M52 Core-based 32-bit Real-time MCU

Version: V1.0

© Geehy Semiconductor Co., Ltd.

1. Product Characteristics

Arm Cortex-M52 32-bit CPU

- 200 MHz operating frequency (Tj: -40 to 150℃)
- IEEE 754 single-precision floating-point unit (FPU)
- Zidian Math Instruction Extension
  - Trigonometric math unit (TMU)
  - CRC engine and instructions (VCRC)
- Nested vectored interrupt controller (NVIC)
- Equipped with Helium™ technology based on the M-profile Vector Extension (MVE)
- Memory protection unit (MPU)
  - Supports 8 configurable regions
- 4KB each for I-Cache and D-Cache

Memory

- 256KB FLASH
  - Two independent 128KB banks
  - ECC protection
  - Supports fast dual-bank code switching (A/B Swap)
- 40KB SRAM
  - ECC protection
- Supports third-party dual-zone security
- Unique identification (UID) number

Clock and System Control

- Two internal zero-pin 10MHz oscillators
- On-chip crystal oscillator and external clock input
- Window watchdog timer module
  - 1 watchdog timer
  - 1 NMIWDT timer
- Clock loss detection circuit
- Dual-clock comparator module (DCCOMP)

1.1V core and 3.3V I/O design

- Built-in 1.1V linear voltage regulator
- Brown-out reset (BOR) circuit

System Peripherals

- 6-channel direct memory access (DMA) controller
- 52 independently programmable multiplexed general-purpose input/output (GPIO) pins (11 shared with analog functions)
- 10 digital inputs (AIO) on analog pins
- Enhanced peripheral interrupt extension (EXTI) module
- Supports multiple low-power modes (LPM) with external wake-up

Communication Peripherals

- 1 power management bus (PMBUS) interface
- 2 inter-integrated circuit (I2C) interfaces
- 2 controller area network (CAN) bus ports
  - 1 port supports CAN FD
- 1 serial peripheral interface (SPI) port
- 3 serial communication interfaces (UART)
- 1 UART-compatible local interconnect network (LIN)

Analog System

- 2 3.72 MSPS 12-bit analog-to-digital converters (ADC)
  - Up to 21 external channels (11 shared with GPIO)
  - Four integrated post-processing blocks (PPB) per ADC
- 4 window comparators (COMP) with 12-bit reference digital-to-analog converters (DAC)
  - Integrated digital filter
- 2 12-bit buffered DAC outputs

Enhanced Control Peripherals

- 14 PWM channels
  - All 14 support high resolution (initial phase deviation between PWM modules within 10ns)

  - Typical resolution of 150ps in high-resolution mode
  - Integrated dead-band support
  - Integrated hardware trip zone (TZ)
- 3 enhanced capture (CAP) modules
- 1 enhanced quadrature encoder pulse (QEP) module supporting CW/CCW operation

Flexible logic block (FLB)

- Enhances existing peripheral functions

Debug System

- SWD / JTAG / cJTAG

Diagnostic Features

- Memory Built-In Self-Test (MBIST)

Related Certifications

- G32R502xCx8 models: AEC-Q100 Grade 1 qualification in progress

Package Options

- LQFP 80，12mm*12mm
- LQFP 64，10mm*10mm
- HTQFP 48，7mm*7mm
- VQFN 32，5mm*5mm

Temperature Options (Ambient Temperature)

- -40℃~105℃ / -40℃~125℃

Applications

- Variable-frequency drive
- Photovoltaic optimizer
- Telecom power supply
- Micro inverter
- Server power module
- DC charging power module
- Other communication module

Contents

1 Product Characteristics 1

2 Product Information 7

2.1 Product Information Table 7

2.2 Product Model Table 9

3 Pin Information 10

3.1 Pin Definition Diagrams 10

3.2 Pin Attributes 14

3.3 Pin Signal Descriptions 44

3.3.1 Analog Signals 44

3.3.2 Digital Signals 48

3.3.3 Power Supply and Grounding 55

3.3.4 Debug and Reset 55

3.4 Pin Multiplexing 57

3.4.1 GPIO Multiplexing Pins 57

3.4.2 Analog Input Pins Multiplexed as Digital Inputs (AIO) 62

3.4.3 Digital Inputs and Outputs on ADC Pins (AGPIO) 62

3.4.4 GPIO Input X-BAR 62

3.4.5 GPIO Output X-BAR, PWM X-BAR, and FLB XBAR 64

3.5 Pins with Internal Pull-up or Pull-down Resistors 64

3.6 Connections for Unused Pins 65

4 Module Description 67

4.1 Introduction 67

4.2 Functional Block Diagram 68

4.3 Memory 69

4.3.1 Memory Map 69

4.3.2 Flash Map 69

4.3.3 Peripheral Register Memory Map 71

4.3.4 Memory Types 73

4.4 Identification 73

4.5 Bus Architecture - Peripheral Connections 74

4.6 Processor 75

4.6.1 Floating-Point Unit (FPU) 75
4.6.2 Zidian Math Instruction Extension - Trigonometric Math Unit (TMU) 75
4.6.3 CRC Engine and Instructions (VCRC) 75
4.6.4 Fast Integer Division Unit (FINTDIV) 76
4.6.5 Helium 76
4.7 Direct Memory Access (DMA) 76
4.8 ROM 80
4.8.1 Boot ROM and Peripheral Boot 80
4.8.2 Entry Addresses 85
4.8.3 MPOST Configuration in GPREG2 85
4.8.4 M-POST Results 86
4.9 Dual-Code Security Module (DCS) 87
4.10 Watchdog 87
4.11 Flexible logic block (FLB) 88
5 Electrical Characteristics 89
5.1 Absolute Maximum Ratings 89
5.2 EMC 90
5.2.1 Electrostatic Discharge Immunity (ESD) 90
5.2.2 Latch up 90
5.3 Recommended Operating Conditions 90
5.4 Power Consumption Summary 91
5.4.1 System Current Consumption - VREG Enabled 91
5.4.2 System Current Consumption - VREG Disabled 92
5.4.3 Current Consumption Graphs 93
5.4.4 Reducing Current Consumption 94
5.5 Electrical Characteristics 94
5.6 Thermal Resistance Characteristics 96
5.7 System 98
5.7.1 Power Management Module (PMM) 98
5.7.2 Reset Timing 106
5.7.3 Clock Specifications 108
5.7.4 Flash Parameters 118

5.7.5 Debug and Emulation 119
5.7.6 GPIO Electrical Data and Timing 122
5.7.7 Interrupts (NVIC and EXTI) 125
5.8 Analog Peripherals 127
5.8.1 Analog Pins and Internal Connections 127
5.8.2 Analog-to-Digital Converter (ADC) 130
5.8.3 Temperature Sensor 137
5.8.4 Buffered Digital-to-Analog Converter (DAC) 137
5.8.5 Comparator (COMP) 143
5.9 Control Peripherals 146
5.9.1 Capture (CAP) 146
5.9.2 Pulse Width Modulator (PWM) 147
5.9.3 High-Resolution Pulse Width Modulator (HRPWM) 148
5.9.4 Quadrature Encoder Pulse (QEP) 149
5.10 Communication Peripherals 150
5.10.1 Controller Area Network (CAN) 150
5.10.2 Controller Area Network with Flexible Data Rate (CAN FD) 151
5.10.3 Inter-Integrated Circuit (I2C) 152
5.10.4 Power Management Bus (PMBUS) Interface 153
5.10.5 Serial Communication Interface (UART) 154
5.10.6 Serial Peripheral Interface (SPI) 155
5.10.7 Local Interconnect Network (LIN) 161
5.11 Dual-Clock Comparator (DCCOMP) 163
5.11.1 Introduction 163
5.11.2 Main Features 163
5.11.3 Block Diagram 163
5.11.4 Functional Description 163
6 Package Information 167
6.1 LQFP80 (12mm*12mm) Package Information 167
6.2 LQFP64 (10mm*10mm) Package Information 170
6.3 HTQFP48 (7mm*7mm) Package Information 173

6.4 VQFN32 (5mm*5mm) Package Information 176
6.5 Package Marking 177

7 Packing Information 179
7.1 Tape Packing 179
7.2 Tray Packing 180

8 Ordering Information 182

9 Common Functional Module Names 184

10 Revision History 185

2. Product Information

2.1. Product Information Table

Refer to the following table for product functions and peripheral configurations.

Table 1 Chip Functions and Peripherals

Product		**G32R502**			
Model		KCUx	CCEx	RCTx	MCTx
Package		VQFN32	HTQFP48	LQFP64	LQFP80
Processor and Accelerators					
CPU: Cortex-M52	Frequency	200MHz			
	FPU	Single-precision FPU support			
	VCRC	Supported			
	TMU	Supported			
6-channel DMA		Supported			
Memory					
Total FLASH capacity		2 x 128KB			
SRAM	ITCM	16KB default, 32KB maximum			
	DTCM	24KB default, 32KB maximum, 8KB minimum			
	Total capacity	40KB			
Flash ECC		Supported			
RAM ECC		Supported			
ROM	BootROM	16KB			
	FLASH API	16KB			
	BootLoader and math library	64KB			
	Total capacity	96KB			
System					
Flexible logic block (FLB)		4			
32-bit CPU timer		3			
Watchdog timer		1			
Non-maskable interrupt watchdog (NMIWDT) Timer		1			
External high-speed crystal		Supported			
Internal high-speed oscillator		2 × 10MHz			
Dual-clock comparator module (DCCOMP)		1			

Product		G32R502			
Model		KCUx	CCEx	RCTx	MCTx
Package		VQFN32	HTQFP48	LQFP64	LQFP80
GPIO pins (1)		18	27	37	52
AIO inputs		6	9	10	10
NVIC		227 interrupt lines 16 levels of interrupt nesting			
Analog Peripherals					
12-bit ADC	Number of ADCs	2			
	Million samples per second	3.72 MSPS			
	Conversion time	268.75 ns			
	ADC channels (single-ended)	11	18	21	21
Temperature sensor (T-sensor)		1			
Window comparator (COMP)		4			
12-bit DAC		2			
Control Peripherals					
CAP modules		3			
PWM/HRPWM channels		14 (all 14 support HRPWM)			
QEP modules		1			
Communication Peripherals					
CAN/CAN FD		2 ports (1 supports CAN FD)			
I2C		2			
UART		3			
SPI		1			
LIN		1			
PMBUS		1			
Voltage					
Operating voltage range		3.1V~3.6V			
Temperature					
Junction temperature (T_J)		–40℃ to 150℃			
Operating ambient temperature (T_A)		-40℃ to 105℃ (Suffix x = 7 devices) or -40℃ to 125℃ (Suffix x = 8 devices)			

Note:

1. Additional information on GPIO pins shared with analog functions:

The 32-pin model provides 18 GPIOs: 5 shared with analog functions and 4 shared with TDI, TDO, X1, and X2;

The 48-pin model provides 27 GPIOs: 9 shared with analog functions and 4 shared with TDI, TDO, X1, and X2;

The 64-pin model provides 37 GPIOs: 11 shared with analog functions and 4 shared with TDI, TDO, X1, and X2;

The 80-pin model provides 52 GPIOs: 11 shared with analog functions and 4 shared with TDI, TDO, X1, and X2.

2.2. Product Model Table

Table 2 Product Model Table

Product model	Product package	Memory configuration	Operating temperature (T_A)	AEC-Q100 standard
G32R502MCT7	LQFP80	Flash 256KB，SRAM 40KB	-40℃~105℃	-
G32R502RCT7	LQFP64			
G32R502CCE7	HTQFP48			
G32R502KCU7	VQFN32			
G32R502MCT8	LQFP80	Flash 256KB，SRAM 40KB	-40℃~125℃	Grade1
G32R502RCT8	LQFP64			
G32R502CCE8	HTQFP48			
G32R502KCU8	VQFN32			

3. Pin Information

3.1. Pin Definition Diagrams

Figure 1 G32R502 Series LQFP80 Pinout

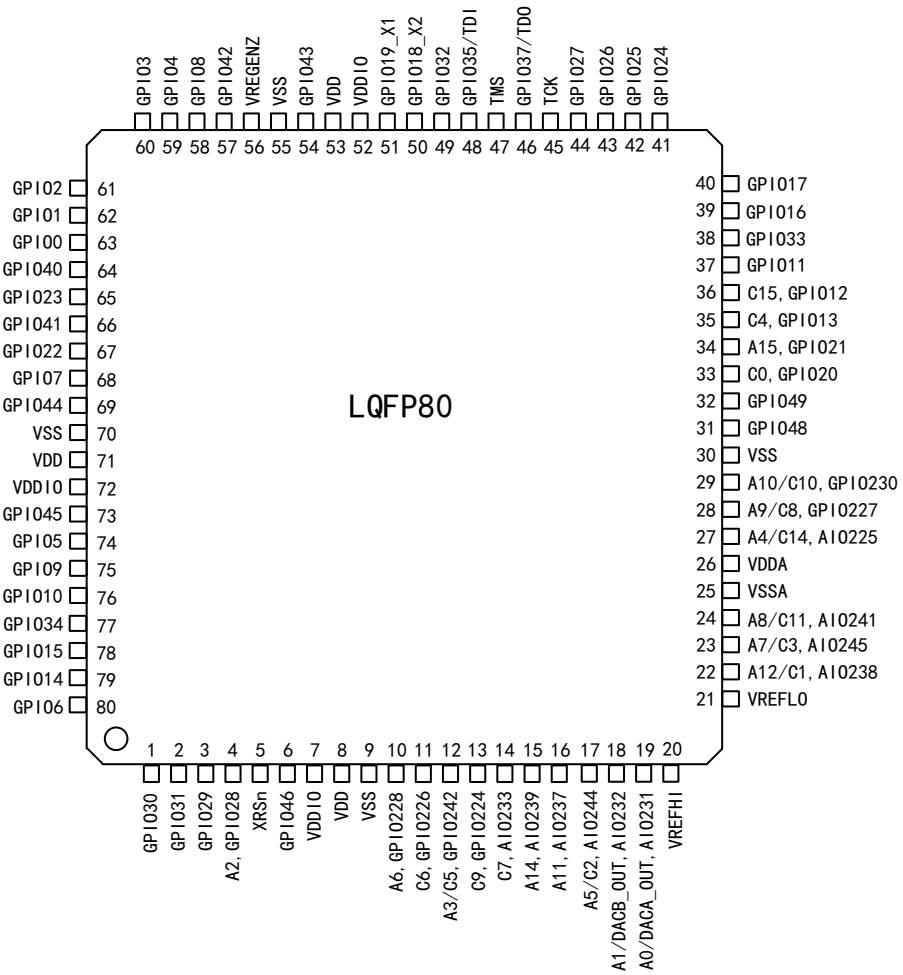


Figure 2 G32R502 Series LQFP64 Pinout

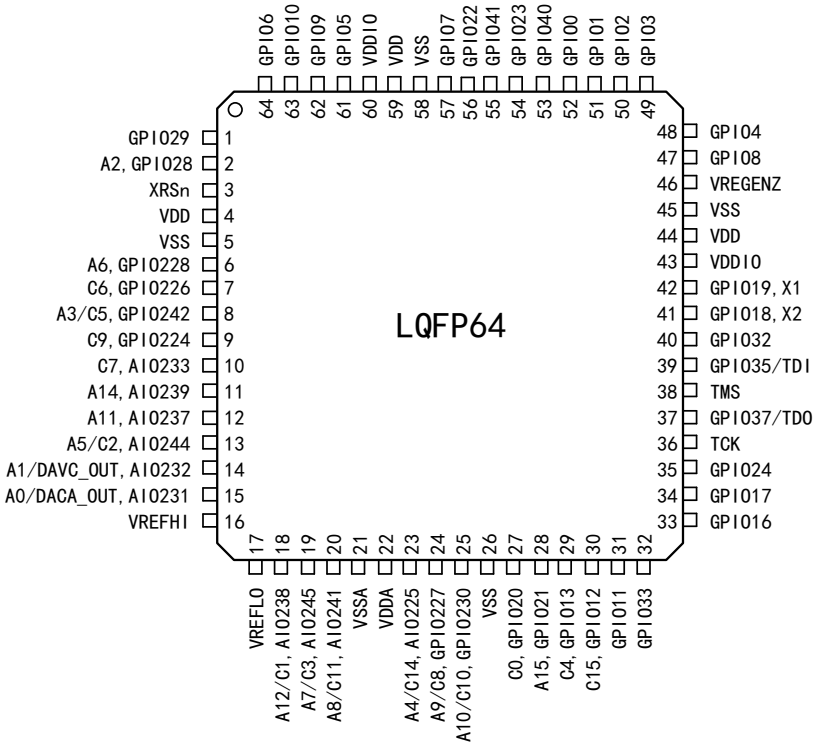


Figure 3 G32R502 Series HTQFP48 Pinout

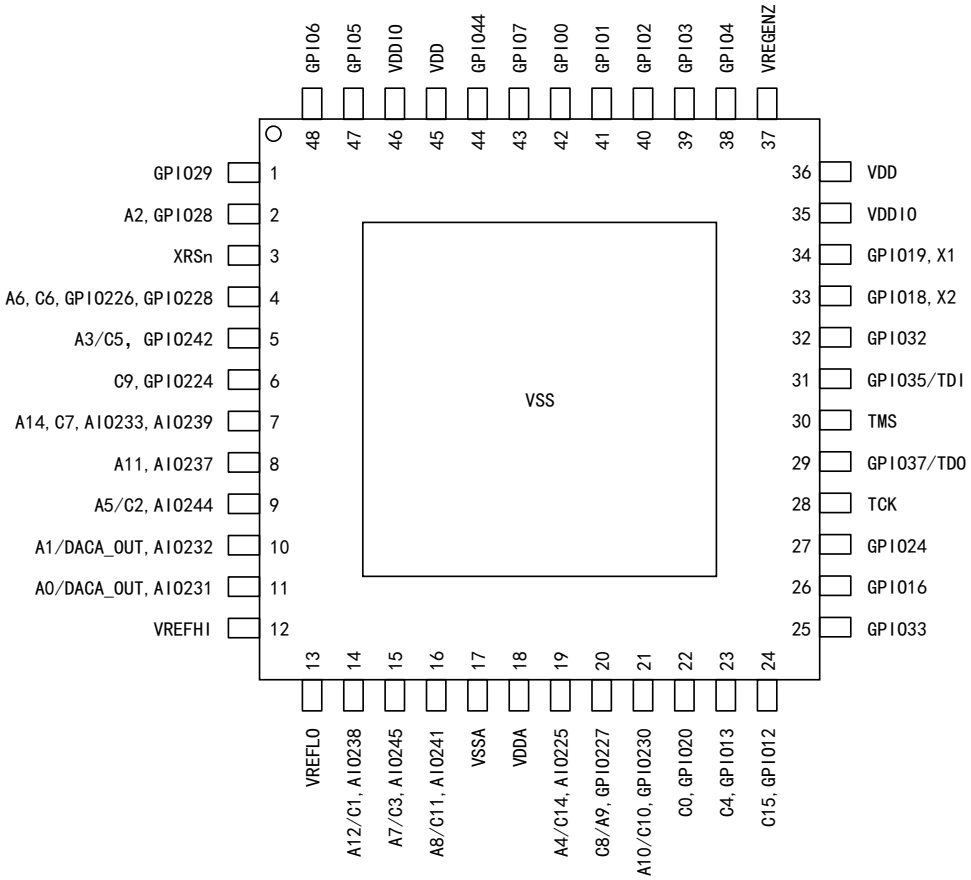
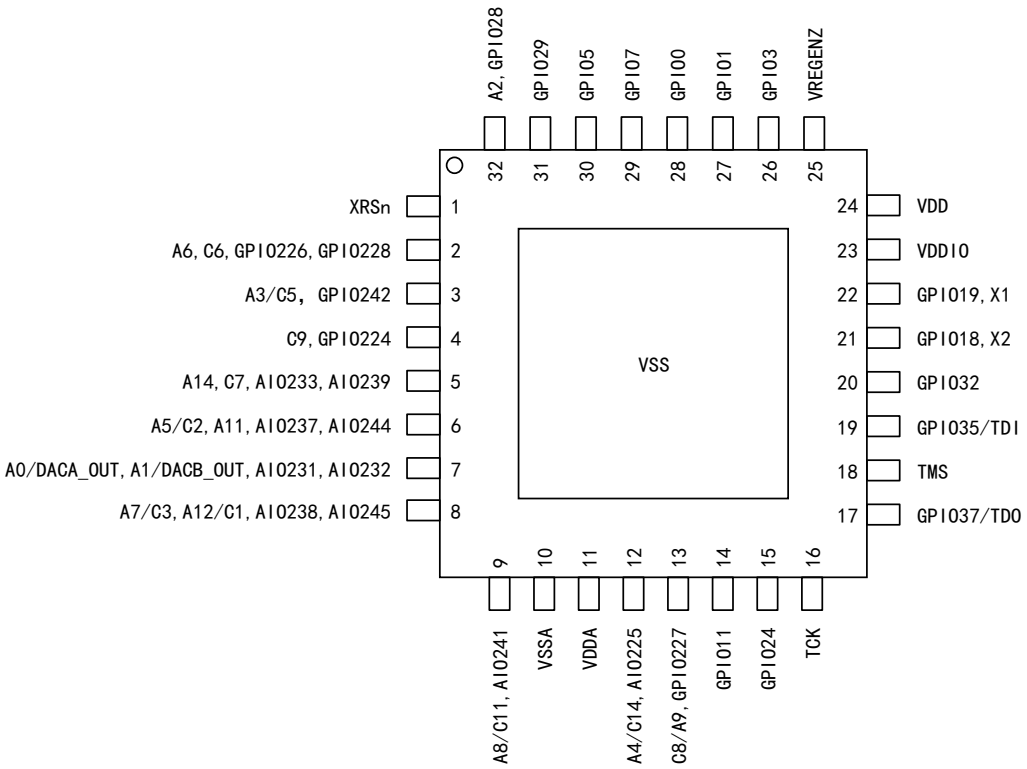


Figure 4 G32R502 Series VQFN32 Pinout



3.2. Pin Attributes

Table 3 Pin Attributes

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
Analog							
A0		19	15	11	7	I	ADC-A input 0
DACA_OUT						O	DAC-A output
COMP3_HP2						I	COMP-3 high comparator positive input 2
COMP3_LP2						I	COMP-3 low comparator positive input 2
AIO231	0, 4, 8, 12					I	Analog pin for digital input 231
A1		18	14	10	7	I	ADC-A input 1
DACB_OUT						O	DAC-B output
COMP1_HP4						I	COMP-1 high comparator positive input 4
COMP1_LP4						I	COMP-1 low comparator positive input 4
AIO232	0, 4, 8, 12					I	Analog pin for digital input 232
C9		13	9	6	4	I	ADC-C input 9
COMP1_HP0						I	COMP-1 high comparator positive input 0
COMP1_LP0						I	COMP-1 low comparator positive input 0
GPIO224						I/O	General-purpose input/output 224. This pin also has digital mux functions, described in the GPIO section of Table 5.

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
A3		12	8	5	3	I	ADC-A input 3
C5						I	ADC-C input 5
COMP3_HN0						I	COMP-3 high comparator negative input 0
COMP3_HP3						I	COMP-3 high comparator positive input 3
COMP3_LN0						I	COMP-3 low comparator negative input 0
COMP3_LP3						I	COMP-3 low comparator positive input 3
GPIO242						I/O	General-purpose input/output 242. This pin also has digital mux functions, described in the GPIO section of Table 5.
A4		27	23	19	12	I	ADC-A input 4
C14						I	ADC-C input 14
COMP2_HP0						I	COMP-2 high comparator positive input 0
COMP2_LP0						I	COMP-2 low comparator positive input 0
COMP4_HN0						I	COMP-4 high comparator negative input 0
COMP4_HP3						I	COMP-4 high comparator positive input 3
COMP4_LN0						I	COMP-4 low comparator negative input 0
COMP4_LP3						I	COMP-4 low comparator positive input 3
AIO225	0, 4, 8, 12					I	Analog pin for digital input 225
A5		17	13	9	6	I	ADC-A input 5
C2						I	ADC-C input 2

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
VDAC						I	Optional external reference voltage for the on-chip digital-to-analog converters. A 100pF capacitor is connected from this pin to VSSA whether the pin is used as an ADC input or a DAC reference. This capacitor cannot be disabled. If the pin is used as a reference, ensure that no large current flows through it.
COMP3_HN1						I	COMP-3 high comparator negative input 1
COMP3_HP1						I	COMP-3 high comparator positive input 1
COMP3_LN1						I	COMP-3 low comparator negative input 1
COMP3_LP1						I	COMP-3 low comparator positive input 1
AIO244	0, 4, 8, 12					I	Analog pin for digital input 244
A6		10	6	4	2	I	ADC-A input 6
COMP1_HP2						I	COMP-1 high comparator positive input 2
COMP1_LP2						I	COMP-1 low comparator positive input 2
GPIO228						I/O	General-purpose input/output 228. This pin also has digital mux functions, described in the GPIO section of Table 5.
A7		23	19	15	8	I	ADC-A input 7
C3						I	ADC-C input 3
COMP4_HN1						I	COMP-4 high comparator negative input 1
COMP4_HP1						I	COMP-4 high comparator positive input 1
COMP4_LN1						I	COMP-4 low comparator negative input 1

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
COMP4_LP1						I	COMP-4 low comparator positive input 1
AIO245	0, 4, 8, 12					I	Analog pin for digital input 245
A8		24	20	16	9	I	ADC-A input 8
C11						I	ADC-C input 11
COMP2_HP4						I	COMP-2 high comparator positive input 4
COMP2_LP4						I	COMP-2 low comparator positive input 4
COMP4_HP4						I	COMP-4 high comparator positive input 4
COMP4_LP4						I	COMP-4 low comparator positive input 4
AIO241	0, 4, 8, 12					I	Analog pin for digital input 241
A10		29	25	21	13	I	ADC-A input 10
C10						I	ADC-C input 10
COMP2_HN0						I	COMP-2 high comparator negative input 0
COMP2_HP3						I	COMP-2 high comparator positive input 3
COMP2_LN0						I	COMP-2 low comparator negative input 0
COMP2_LP3						I	COMP-2 low comparator positive input 3
GPIO230						I/O	General-purpose input/output 230. This pin also has digital mux functions, described in the GPIO section of Table 5.
A11		16	12	8	6	I	ADC-A input 11
COMP1_HN1						I	COMP-1 high comparator negative input 1

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
COMP1_HP1						I	COMP-1 high comparator positive input 1
COMP1_LN1						I	COMP-1 low comparator negative input 1
COMP1_LP1						I	COMP-1 low comparator positive input 1
AIO237	0, 4, 8, 12					I	Analog pin for digital input 237
A12		22	18	14	8	I	ADC-A input 12
C1						I	ADC-C input 1
COMP2_HN1						I	COMP-2 high comparator negative input 1
COMP2_HP1						I	COMP-2 high comparator positive input 1
COMP2_LN1						I	COMP-2 low comparator negative input 1
COMP2_LP1						I	COMP-2 low comparator positive input 1
COMP4_HP2						I	COMP-4 high comparator positive input 2
COMP4_LP2						I	COMP-4 low comparator positive input 2
AIO238	0, 4, 8, 12					I	Analog pin for digital input 238
C7		14	10	7	5	I	ADC-C input 7
COMP1_HN0						I	COMP-1 high comparator negative input 0
COMP1_HP3						I	COMP-1 high comparator positive input 3
COMP1_LN0						I	COMP-1 low comparator negative input 0
COMP1_LP3						I	COMP-1 low comparator positive input 3

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
AIO233	0, 4, 8, 12					I	Analog pin for digital input 233
A2		4	2	2	32	I	ADC-A input 2
GPIO28						I/O	General-purpose input/output 28. This pin also has digital mux functions, described in the GPIO section of Table 5. Note: GPIO28 and comparator 4 (COMP4) cannot be used simultaneously.
C0		33	27	22		I	ADC-C input 0
GPIO20						I/O	General-purpose input/output 20. This pin also has digital mux functions, described in the GPIO section of Table 5.
A15		34	28			I	ADC-A input 15
GPIO21						I/O	General-purpose input/output 21. This pin also has digital mux functions, described in the GPIO section of Table 5.
C4		35	29	23		I	ADC-C input 4
GPIO13						I/O	General-purpose input/output 13. This pin also has digital mux functions, described in the GPIO section of Table 5.
C15		36	30	24		I	ADC-C input 15
GPIO12						I/O	General-purpose input/output 12. This pin also has digital mux functions, described in the GPIO section of Table 5.
A14		15	11	7	5	I	ADC-A input 14
COMP3_HP4						I	COMP-3 high comparator positive input 4
COMP3_LP4						I	COMP-3 low comparator positive input 4

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
AIO239	0, 4, 8, 12					I	Analog pin for digital input 239
C6		11	7	4	2	I	ADC-C input 6
COMP3_HP0						I	COMP-3 high comparator positive input 0
COMP3_LP0						I	COMP-3 low comparator positive input 0
GPIO226						I/O	General-purpose input/output 226. This pin also has digital mux functions, described in the GPIO section of Table 5.
A9		28	24	20	13	I	ADC-A input 9
C8						I	ADC-C input 8
COMP2_HP2						I	COMP-2 high comparator positive input 2
COMP2_LP2						I	COMP-2 low comparator positive input 2
COMP4_HP0						I	COMP-4 high comparator positive input 0
COMP4_LP0						I	COMP-4 low comparator positive input 0
GPIO227						I/O	General-purpose input/output 227. This pin also has digital mux functions, described in the GPIO section of Table 5.
VREFHI		20	16	12		I	ADC high reference voltage. In external reference mode, drive this pin externally with the high reference voltage. In internal reference mode, the device drives the voltage onto this pin. In either mode, place a capacitor of at least 2.2μF on this pin. Place it between VREFHI and VREFLO as close to the device as possible. On the VQFN32 package, VREFHI is internally connected to VDDA.
VREFLO		21	17	13		I	ADC low reference voltage

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
GPIO							
GPIO0	0, 4, 8, 12	63	52	42	28	I/O	General-purpose input/output 0
PWM1_A	1					O	PWM-1 output A
CANA_RX	2					I	CAN-A receive
OUTPUTXBAR7	3					O	Output X-BAR output 7
UARTA_RX	5					I	UART-A receive data
I2CA_SDA	6					I/OD	I2C-A open-drain bidirectional data
SPIA_STE	7					I/O	SPI-A slave transmit enable (STE)
CANFDA_RX	10					I	CAN/CAN FD-A receive
QEP1_INDEX	13					I/O	QEP-1 index
PWM3_A	15					O	PWM-3 output A
GPIO1	0, 4, 8, 12	62	51	41	27	I/O	General-purpose input/output 1
PWM1_B	1					O	PWM-1 output B
UARTA_TX	5					O	UART-A transmit data
I2CA_SCL	6					I/OD	I2C-A open-drain bidirectional clock
SPIA_SOMI	7					I/O	SPI-A slave output, master input (SOMI)
QEP1_STROBE	9					I/O	QEP-1 strobe
CANFDA_TX	10					O	CAN/CAN FD-A transmit

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
PWM3_B	15					O	PWM-3 output B
GPIO2	0, 4, 8, 12	61	50	40		I/O	General-purpose input/output 2
PWM2_A	1					O	PWM-2 output A
OUTPUTXBAR1	5					O	Output X-BAR output 1
PMBUSA_SDA	6					I/OD	PMBUS-A open-drain bidirectional data
SPIA_SIMO	7					I/O	SPI-A slave input, master output (SIMO)
UARTA_TX	9					O	UART-A transmit data
I2CB_SDA	11					I/OD	I2C-B open-drain bidirectional data
CANA_TX	14					O	CAN-A transmit
PWM4_A	15					O	PWM-4 output A
GPIO3	0, 4, 8, 12	60	49	39	26	I/O	General-purpose input/output 3
PWM2_B	1					O	PWM-2 output B
OUTPUTXBAR2	2/5					O	Output X-BAR output 2
PMBUSA_SCL	6					I/OD	PMBUS-A open-drain bidirectional clock
SPIA_CLK	7					I/O	SPI-A clock
UARTA_RX	9					I	UART-A receive data
I2CB_SCL	11					I/OD	I2C-B open-drain bidirectional clock
CANA_RX	14					I	CAN-A receive

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
PWM4_B	15					O	PWM-4 output B
GPIO4	0, 4, 8, 12	59	48	38		I/O	General-purpose input/output 4
PWM3_A	1					O	PWM-3 output A
I2CA_SCL	2					I/OD	I2C-A open-drain bidirectional clock
CANFDA_TX	3					O	CAN/CANFD-A transmit
OUTPUTXBAR3	5					O	Output X-BAR output 3
CANA_TX	6					O	CAN-A transmit
SPIA_SOMI	14					I/O	SPI-A slave output, master input (SOMI)
PWM1_A	15					O	PWM-1 output A
GPIO5	0, 4, 8, 12	74	61	47	30	I/O	General-purpose input/output 5
PWM3_B	1					O	PWM-3 output B
I2CA_SDA	2					I/OD	I2C-A open-drain bidirectional data
OUTPUTXBAR3	3					O	Output X-BAR output 3
CANFDA_RX	5					I	CAN/CANFD-A receive
CANA_RX	6					I	CAN-A receive
SPIA_STE	7					I/O	SPI-A slave transmit enable (STE)
UARTA_RX	11					I	UART-A receive data
PWM1_B	15					O	PWM-1 output B

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
GPIO6	0, 4, 8, 12	80	64	48		I/O	General-purpose input/output 6
PWM4_A	1					O	PWM-4 output A
OUTPUTXBAR4	2					O	Output X-BAR output 4
SYNCOUT	3					O	External PWM synchronization pulse
QEP1_A	5					I	QEP-1 input A
PWM2_A	15					O	PWM-2 output A
GPIO7	0, 4, 8, 12	68	57	43	29	I/O	General-purpose input/output 7
PWM4_B	1					O	PWM-4 output B
PWM2_A	2					O	PWM-2 output A
OUTPUTXBAR5	3					O	Output X-BAR output 5
QEP1_B	5					I	QEP-1 input B
SPIA_SIMO	7					I/O	SPI-A slave input, master output (SIMO)
UARTA_TX	11					O	UART-A transmit data
CANA_TX	14					O	CAN-A transmit
PWM2_B	15					O	PWM-2 output B
GPIO8	0, 4, 8, 12	58	47			I/O	General-purpose input/output 8
PWM5_A	1					O	PWM-5 output A
ADCSOCAO	3					O	ADC start-of-conversion A for an external ADC

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
QEP1_STROBE	5					I/O	QEP-1 strobe
UARTA_TX	6					O	UART-A transmit data
SPIA_SIMO	7					I/O	SPI-A slave input, master output (SIMO)
I2CA_SCL	9					I/OD	I2C-A open-drain bidirectional clock
GPIO9	0, 4, 8, 12	75	62			I/O	General-purpose input/output 9
PWM5_B	1					O	PWM-5 output B
UARTB_TX	2					O	UART-B transmit data
OUTPUTXBAR6	3					O	Output X-BAR output 6
QEP1_INDEX	5					I/O	QEP-1 index
UARTA_RX	6					I	UART-A receive data
SPIA_CLK	7					I/O	SPI-A clock
I2CB_SCL	14					I/OD	I2C-B open-drain bidirectional clock
GPIO10	0, 4, 8, 12	76	63			I/O	General-purpose input/output 10
PWM6_A	1					O	PWM-6 output A
ADCSOCBO	3					O	ADC start-of-conversion B for an external ADC
QEP1_A	5					I	QEP-1 input A
UARTB_TX	6					O	UART-B transmit data
SPIA_SOMI	7					I/O	SPI-A slave output, master input (SOMI)

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
I2CA_SDA	9					I/OD	I2C-A open-drain bidirectional data
GPIO11	0, 4, 8, 12	37	31		14	I/O	General-purpose input/output 11
PWM6_B	1					O	PWM-6 output B
CANA_RX	2					I	CAN-A receive
OUTPUTXBAR7	3					O	Output X-BAR output 7
QEP1_B	5					I	QEP-1 input B
UARTB_RX	6					I	UART-B receive data
SPIA_STE	7					I/O	SPI-A slave transmit enable (STE)
SPIA_SIMO	13					I/O	SPI-A slave input, master output (SIMO)
GPIO12	0, 4, 8, 12	36	30	24		I/O	General-purpose input/output 12. This pin also has analog functions, described in the Analog section of Table 4.
PWM7_A	1					O	PWM-7 output A
CANFDA_RX	3					I	CAN/CANFD-A receive
QEP1_STROBE	5					I/O	QEP-1 strobe
UARTB_TX	6					O	UART-B transmit data
PMBUSA_CTL	7					I/O	PMBUS-A control signal - slave input/master output
SPIA_CLK	11					I/O	SPI-A clock
CANA_RX	13					I	CAN-A receive
TRACED2	15					O	TRACE synchronous data output 2

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
GPIO13	0, 4, 8, 12	35	29	23		I/O	General-purpose input/output 13. This pin also has analog functions, described in the Analog section of Table 4.
PWM7_B	1					O	PWM-7 output B
CANFDA_TX	3					OI/O	CAN/CAN FD-A transmit
QEP1_INDEX	5					I	QEP-1 index
UARTB_RX	6					I/OD	UART-B receive data
PMBUSA_ALERT	7					I/O	PMBUS-A open-drain bidirectional alert signal
SPIA_SOMI	11					O	SPI-A slave output, master input (SOMI)
CANA_TX	13					O	CAN-A transmit
TRACED3	15					O	TRACE synchronous data output 3
GPIO14	0, 4, 8, 12	79				I/O	General-purpose input/output 14
UARTB_TX	2					O	UART-B transmit data
I2CB_SDA	5					I/OD	I2C-B open-drain bidirectional data
OUTPUTXBAR3	6					O	Output X-BAR output 3
PMBUSA_SDA	7					I/OD	PMBUS-A open-drain bidirectional data
PWM3_A	13					O	PWM-3 output A
GPIO15	0, 4, 8, 12	78				I/O	General-purpose input/output 15
UARTB_RX	2					I	UART-B receive data
I2CB_SCL	5					I/OD	I2C-B open-drain bidirectional clock

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
OUTPUTXBAR4	6					O	Output X-BAR output 4
PMBUSA_SCL	7					I/OD	PMBUS-A open-drain bidirectional clock
PWM3_B	13					O	PWM-3 output B
GPIO16	0, 4, 8, 12	39	33	26		I/O	General-purpose input/output 16
SPIA_SIMO	1					I/O	SPI-A slave input, master output (SIMO)
OUTPUTXBAR7	3					O	Output X-BAR output 7
PWM5_A	5					O	PWM-5 output A
UARTA_TX	6					O	UART-A transmit data
QEP1_STROBE	9					I/O	QEP-1 strobe
PMBUSA_SCL	10					I/OD	PMBUS-A open-drain bidirectional clock
XCLKOUT	11					O	External clock output. This pin outputs a divided version of the selected clock signal from the device.
TRACED0	15					O	TRACE synchronous data output 0
GPIO17	0, 4, 8, 12	40	34			I/O	General-purpose input/output 17
SPIA_SOMI	1					I/O	SPI-A slave output, master input (SOMI)
OUTPUTXBAR8	3					O	Output X-BAR output 8
PWM5_B	5					O	PWM-5 output B
UARTA_RX	6					I	UART-A receive data
QEP1_INDEX	9					I/O	QEP-1 index

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
PMBUSA_SDA	10					I/OD	PMBUS-A open-drain bidirectional data
CANA_TX	11					O	CAN-A transmit
PWM6_A	14					O	PWM-6 output A
TRGIO	15					I/O	External bidirectional trigger
GPIO18	0, 4, 8, 12	50	41	33	21	I/O	General-purpose input/output 18
SPIA_CLK	1					I/O	SPI-A clock
UARTB_TX	2					O	UART-B transmit data
CANA_RX	3					I	CAN-A receive
PWM6_A	5					O	PWM-6 output A
I2CA_SCL	6					I/OD	I2C-A open-drain bidirectional clock
PMBUSA_CTL	10					I/O	PMBUS-A control signal - slave input/master output
XCLKOUT	11					O	External clock output. This pin outputs a divided version of the selected clock signal from the device.
X2	ALT					I/O	Crystal oscillator output.
GPIO19	0, 4, 8, 12	51	42	34	22	I/O	General-purpose input/output 19
SPIA_STE	1					I/O	SPI-A slave transmit enable (STE)
UARTB_RX	2					I	UART-B receive data
CANA_TX	3					O	CAN-A transmit
PWM6_B	5					O	PWM-6 output B

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
I2CA_SDA	6					I/OD	I2C-A open-drain bidirectional data
PMBUSA_ALERT	10					I/OD	PMBUS-A open-drain bidirectional alert signal
X1	ALT					I/O	Crystal oscillator or single-ended clock input. Device initialization software must configure this pin before enabling the crystal oscillator. To use this oscillator, connect a quartz crystal circuit to X1 and X2. This pin can also accept a single-ended 3.3V clock.
ExtR	ALT2					I	External resistor for the internal oscillator. This can improve clock accuracy.
GPIO20	0, 4, 8, 12	33	27	22		I/O	General-purpose input/output 20. This pin also has analog functions, described in the Analog section of Table 4.
QEP1_A	1					I	QEP-1 input A
CANA_TX	3					O	CAN-A transmit
SPIA_SIMO	6					I/O	SPI-A slave input, master output (SIMO)
CANFDA_TX	9					O	CAN/CANFD-A transmit
I2CA_SCL	11					I/OD	I2C-A open-drain bidirectional clock
UARTC_TX	15					O	UART-C transmit data
GPIO21	0, 4, 8, 12	34	28			I/O	General-purpose input/output 21. This pin also has analog functions, described in the Analog section of Table 4.
QEP1_B	1					I	QEP-1 input B
CANA_RX	3					I	CAN-A receive
SPIA_SOMI	6					I/O	SPI-A slave output, master input (SOMI)

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
CANFDA_RX	9					I	CAN/CANFD-A receive
I2CA_SDA	11					I/OD	I2C-A open-drain bidirectional data
UARTC_RX	15					I	UART-C receive data
GPIO22	0, 4, 8, 12	67	56			I/OI/O	General-purpose input/output 22
QEP1_STROBE	1					O	QEP-1 strobe
UARTB_TX	3					O	UART-B transmit data
LINA_TX	9					O	LIN-A transmit
PWM4_A	14						PWM-4 output A
GPIO23	0, 4, 8, 12	65	54			I/O	General-purpose input/output 23
QEP1_INDEX	1					I/O	QEP-1 index
UARTB_RX	3					I	UART-B receive data
LINA_RX	9					I	LIN-A receive
PWM4_B	14					O	PWM-4 output B
GPIO24	0, 4, 8, 12	41	35	27	15	I/OO	General-purpose input/output 24
OUTPUTXBAR1	1					I	Output X-BAR output 1
SPIA_STE	3					O	SPI-A slave transmit enable (STE)
PWM4_A	5					I/O	PWM-4 output A
SPIA_SIMO	6					I/OD	SPI-A slave input, master output (SIMO)

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
PMBUSA_SCL	10					O	PMBUS-A open-drain bidirectional clock
UARTA_TX	11					O	UART-A transmit data
ERRORSTS	13					O	Error status output. This signal requires an external pull-down resistor.
GPIO25	0, 4, 8, 12	42				I/O	General-purpose input/output 25
OUTPUTXBAR2	1					O	Output X-BAR output 2
QEP1_A	5					I	QEP-1 input A
PMBUSA_SDA	10					I/OD	PMBUS-A open-drain bidirectional data
UARTA_RX	11					I	UART-A receive data
GPIO26	0, 4, 8, 12	43				I/O	General-purpose input/output 26
OUTPUTXBAR3	1,5					O	Output X-BAR output 3
PMBUSA_CTL	10					I/O	PMBUS-A control signal - slave input/master output
I2CA_SDA	11					I/OD	I2C-A open-drain bidirectional data
GPIO27	0, 4, 8, 12	44				I/O	General-purpose input/output 27
OUTPUTXBAR4	1,5					O	Output X-BAR output 4
PMBUSA_ALERT	10					I/OD	PMBUS-A open-drain bidirectional alert signal
I2CA_SCL	11					I/OD	I2C-A open-drain bidirectional clock
GPIO28	0, 4, 8, 12	4	2	2	32	I/O	General-purpose input/output 28. This pin also has analog functions, described in the Analog section of Table 4.

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
							Note: GPIO28 and COMP4 cannot be used simultaneously.
UARTA_RX	1					I	UART-A receive data
PWM7_A	3					O	PWM-7 output A
OUTPUTXBAR5	5					O	Output X-BAR output 5
QEP1_A	6					I	QEP-1 input A
LINA_TX	10					O	LIN-A transmit
SPIA_CLK	11					I/O	SPI-A clock
ERRORSTS	13					O	Error status output. This signal requires an external pull-down resistor.
I2CB_SDA	14					I/OD	I2C-B open-drain bidirectional data
TRACECLK	15					O	TRACE clock
GPIO29	0, 4, 8, 12	3	1	1	31	I/O	General-purpose input/output 29
UARTA_TX	1					O	UART-A transmit data
PWM7_B	3					O	PWM-7 output B
OUTPUTXBAR6	5					O	Output X-BAR output 6
QEP1_B	6					I	QEP-1 input B
LINA_RX	10					I	LIN-A receive
SPIA_STE	11					I/O	SPI-A slave transmit enable (STE)
ERRORSTS	13					O	Error status output. This signal requires an external pull-down

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
							resistor.
I2CB_SCL	14					I/OD	I2C-B open-drain bidirectional clock
TRACED2	15					O	TRACE synchronous data output 2
GPIO30	0, 4, 8, 12	1				I/O	General-purpose input/output 30
CANA_RX	1					I	CAN-A receive
OUTPUTXBAR7	5					O	Output X-BAR output 7
QEP1_STROBE	6					I/O	QEP-1 strobe
CANFDA_RX	10					I	CAN/CANFD-A receive
PWM1_A	11					O	PWM-1 output A
TRACED1	15					O	TRACE synchronous data output 1
GPIO31	0, 4, 8, 12	2				I/O	General-purpose input/output 31
CANA_TX	1					O	CAN-A transmit
OUTPUTXBAR8	5					O	Output X-BAR output 8
QEP1_INDEX	6					I/O	QEP-1 index
CANFDA_TX	10					O	CAN/CANFD-A transmit
PWM1_B	11					O	PWM-1 output B
TRACECLK	15					O	TRACE clock
GPIO32	0, 4, 8, 12	49	40	32	20	I/O	General-purpose input/output 32

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
I2CA_SDA	1					I/OD	I2C-A open-drain bidirectional data
QEP1_INDEX	2					I/O	QEP-1 index
SPIA_CLK	3					I/O	SPI-A clock
PWM4_B	5					O	PWM-4 output B
LINA_TX	6					O	LIN-A transmit
CANA_TX	10					O	CAN-A transmit
PMBUSA_SDA	11					I/OD	PMBUS-A open-drain bidirectional data
ADCSOCBO	13					O	ADC start-of-conversion B for an external ADC
TRGIO	15					I/O	External bidirectional trigger
GPIO33	0, 4, 8, 12	38	32	25		I/O	General-purpose input/output 33
I2CA_SCL	1					I/OD	I2C-A open-drain bidirectional clock
OUTPUTXBAR4	5					O	Output X-BAR output 4
LINA_RX	6					I	LIN-A receive
CANA_RX	10					I	CAN-A receive
ADCSOCAO	13					O	ADC start-of-conversion A for an external ADC
TRACED1	15					O	TRACE synchronous data output 1
GPIO34	0, 4, 8, 12	77				I/O	General-purpose input/output 34
OUTPUTXBAR1	1					O	Output X-BAR output 1

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
PMBUSA_SDA	6					I/OD	PMBUS-A open-drain bidirectional data
I2CB_SDA	14					I/OD	I2C-B open-drain bidirectional data
TRACED3	15					O	TRACE synchronous data output 3
GPIO35	0, 4, 8, 12	48	39	31	19	I/O	General-purpose input/output 35
UARTA_RX	1					I	UART-A receive data
SPIA_SOMI	2					I/O	SPI-A slave output, master input (SOMI)
I2CA_SDA	3					I/OD	I2C-A open-drain bidirectional data
CANA_RX	5					I	CAN-A receive
PMBUSA_SCL	6					I/OD	PMBUS-A open-drain bidirectional clock
LINA_RX	7					I	LIN-A receive
QEP1_A	9					I	QEP-1 input A
PMBUSA_CTL	10					I/O	PMBUS-A control signal - slave input/master output
PWM5_B	11					O	PWM-5 output B
TDI	15					I	JTAG test data input (TDI). TDI is the default mux selection for this pin. The internal pull-up resistor is disabled by default. When using this pin as JTAG TDI, enable the internal pull-up or add an external pull-up resistor on the board to prevent a floating input.
GPIO37	0, 4, 8, 12	46	37	29	17	I/O	General-purpose input/output 37
OUTPUTXBAR2	1					O	Output X-BAR output 2

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
SPIA_STE	2					I/O	SPI-A slave transmit enable (STE)
I2CA_SCL	3					I/OD	I2C-A open-drain bidirectional clock
UARTA_TX	5					O	UART-A transmit data
CANA_TX	6					O	CAN-A transmit
LINA_TX	7					O	LIN-A transmit
QEP1_B	9					I	QEP-1 input B
PMBUSA_ALERT	10					I/OD	PMBUS-A open-drain bidirectional alert signal
PWM5_A	11					O	PWM-5 output A
TDO	15					O	JTAG test data output (TDO). TDO is the default mux selection for this pin. The internal pull-up resistor is disabled by default. When JTAG is inactive, TDO is in the high-impedance state and the pin floats. Enable the internal pull-up or add an external pull-up resistor on the board to prevent a floating GPIO input.
GPIO40	0, 4, 8, 12	64	53			I/O	General-purpose input/output 40
PWM2_B	5					O	PWM-2 output B
PMBUSA_SDA	6					I/OD	PMBUS-A open-drain bidirectional data
UARTB_TX	9					O	UART-B transmit data
QEP1_A	10					I	QEP-1 input A
GPIO41	0, 4, 8, 12	66	55			I/O	General-purpose input/output 41

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
PWM7_A	1					O	PWM-7 output A
PWM2_A	5					O	PWM-2 output A
PMBUSA_SCL	6					I/OD	PMBUS-A open-drain bidirectional clock
UARTB_RX	9					I	UART-B receive data
QEP1_B	10					I	QEP-1 input B
GPIO42	0, 4, 8, 12	57				I/O	General-purpose input/output 42
LINA_RX	2					I	LIN-A receive
OUTPUTXBAR5	3					O	Output X-BAR output 5
PMBUSA_CTL	5					I/O	PMBUS-A control signal - slave input/master output
I2CA_SDA	6					I/OD	I2C-A open-drain bidirectional data
UARTC_RX	7					I	UART-C receive data
QEP1_STROBE	10					I/O	QEP-1 strobe
GPIO43	0, 4, 8, 12	54				I/O	General-purpose input/output 43
OUTPUTXBAR6	3					O	Output X-BAR output 6
PMBUSA_ALERT	5/9					I/OD	PMBUS-A open-drain bidirectional alert signal
I2CA_SCL	6					I/OD	I2C-A open-drain bidirectional clock
UARTC_TX	7					O	UART-C transmit data
QEP1_INDEX	10					I/O	QEP-1 index

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
GPIO44	0, 4, 8, 12	69		44		I/O	General-purpose input/output 44
OUTPUTXBAR7	3					O	Output X-BAR output 7
QEP1_A	5					I	QEP-1 input A
PMBUSA_SDA	6					I/OD	PMBUS-A open-drain bidirectional data
PMBUSA_CTL	9					I/O	PMBUS-A control signal - slave input/master output
GPIO45	0, 4, 8, 12	73				I/O	General-purpose input/output 45
OUTPUTXBAR8	3					O	Output X-BAR output 8
PMBUSA_ALERT	9					I/OD	PMBUS-A open-drain bidirectional alert signal
GPIO46	0, 4, 8, 12	6				I/O	General-purpose input/output 46
LINA_TX	3					O	LIN-A transmit
CANFDA_TX	5					O	CAN/CANFD-A transmit
PMBUSA_SDA	9					I/OD	PMBUS-A open-drain bidirectional data
GPIO48	0, 4, 8, 12	31				I/O	General-purpose input/output 48
OUTPUTXBAR3	1					O	Output X-BAR output 3
CANA_TX	3					O	CAN-A transmit
CANFDA_TX	5					O	CAN/CANFD-A transmit
UARTA_TX	6					O	UART-A transmit data
PMBUSA_SDA	9					I/OD	PMBUS-A open-drain bidirectional data

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
GPIO49	0, 4, 8, 12	32				I/O	General-purpose input/output 49
OUTPUTXBAR4	1					O	Output X-BAR output 4
CANA_RX	3					I	CAN-A receive
CANFDA_RX	5					I	CAN/CANFD-A receive
UARTA_RX	6					I	UART-A receive data
LINA_RX	9					I	LIN-A receive
GPIO224	0, 4, 8, 12	13	9	6	4	I/O	General-purpose input/output 224. This pin also has analog functions, described in the Analog section of Table 4.
OUTPUTXBAR3	5					O	Output X-BAR output 3
SPIA_SIMO	6					I	SPI-A slave input, master output (SIMO)
PWM1_A	9					O	PWM-1 output A
CANA_TX	10					O	CAN-A transmit
QEP1_A	11					I	QEP-1 input A
UARTC_TX	14					O	UART-C transmit data
GPIO226	0, 4, 8, 12	11	7	4	2	I/O	General-purpose input/output 226. This pin also has analog functions, described in the Analog section of Table 4.
LINA_RX	3					I	LIN-A receive
PWM6_A	5					O	PWM-6 output A
SPIA_CLK	6					I/O	SPI-A clock

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
PWM1_B	9					O	PWM-1 output B
QEP1_STROBE	11					I/O	QEP-1 strobe
UARTC_RX	14					I	UART-C receive data
GPIO227	0, 4, 8, 12	28	24	20	13	I/O	General-purpose input/output 227. This pin also has analog functions, described in the Analog section of Table 4.
I2CB_SCL	1					I/OD	I2C-B open-drain bidirectional clock
PWM3_A	3					O	PWM-3 output A
OUTPUTXBAR1	5					O	Output X-BAR output 1
PWM2_B	6					O	PWM-2 output B
GPIO228	0, 4, 8, 12	10	6	4	2	I/O	General-purpose input/output 228. This pin also has analog functions, described in the Analog section of Table 4.
ADCSOCAO	3					O	ADC start-of-conversion A for an external ADC
CANA_TX	5					O	CAN-A transmit
SPIA_SOMI	6					I/O	SPI-A slave output, master input (SOMI)
PWM2_B	9					O	PWM-2 output B
QEP1_B	11					I	QEP-1 input B
GPIO230	0, 4, 8, 12	29	25	21	13	I/O	General-purpose input/output 230. This pin also has analog functions, described in the Analog section of Table 4.
I2CB_SDA	1					I/OD	I2C-B open-drain bidirectional data
PWM3_B	3					O	PWM-3 output B

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
CANA_RX	5					I	CAN-A receive
PWM2_A	6					O	PWM-2 output A
I2CA_SDA	7					I/OD	I2C-A open-drain bidirectional data
PMBUSA_SCL	9					I/OD	PMBUS-A open-drain bidirectional clock
GPIO242	0, 4, 8, 12	12	8	5	3	I/O	General-purpose input/output 242. This pin also has analog functions, described in the Analog section of Table 4.
OUTPUTXBAR2	5					O	Output X-BAR output 2
SPIA_STE	6					I	SPI-A slave transmit enable (STE)
PWM4_A	9					I/O	PWM-4 output A
CANA_RX	10					I	CAN-A receive
QEP1_INDEX	11					I/O	QEP-1 index
Test, JTAG, and Reset							
TCK		45	36	28	16	I	JTAG test clock with an internal pull-up resistor.
TMS		47	38	30	18	I/O	JTAG test mode select (TMS) with an internal pull-up resistor. This serial control input is clocked into the TAP controller on the rising edge of TCK. The device has no TRSTn pin. Place an external pull-up resistor (2.2kΩ recommended) between TMS and VDDIO to keep JTAG in reset during normal operation.
XRSn		5	3	3	1	I/OD	Device reset (input) and watchdog reset (output). The device drives this pin low at power-up. External circuitry can also drive this pin to reset the device. The MCU also drives it low during a watchdog

Signal name	Multiplexer location	LQFP80	LQFP64	HTQFP48	VQFN32	Pin type	Description
							reset. During watchdog reset, XRSn is held low for the watchdog reset duration of 810 OSCCLK cycles. Place a 2.2kΩ to 10kΩ resistor between XRSn and VDDIO. If a noise-filtering capacitor is connected between XRSn and VSS, its capacitance must be 100nF or less. These values allow the watchdog to drive XRSn correctly to VOL within 810 OSCCLK cycles when watchdog reset is asserted. This pin is an open-drain output with an internal pull-up. Use an open-drain device if the pin is driven externally.
Power Supply and Grounding							
VDD		8/53/71	4/44/59	36/45	24		1.1V digital logic supply pin. See the Power Management Module (PMM) section for usage details.
VDDA		26	22	18	11		3.3V analog supply pin. Place a decoupling capacitor of at least 2.2μF on each pin. On the VQFN32 package, VREFHI is internally connected to VDDA. See the PMM section for usage details.
VDDIO		7/52/72	43/60	35/46	23		3.3V digital I/O supply pin. See the PMM section for usage details.
VREGENZ		56	46	37	25	I	Internal voltage regulator enable with an internal pull-down resistor. Connect low to VSS to enable the internal VREG. Connect high to VDDIO to use an external supply.
VSS		9/30/55/70	5/26/45/58	PAD	PAD		Digital ground. For VQFN packages, solder the ground pad on the bottom of the package to the PCB ground plane.
VSSA		25	21	17	10		Analog ground

3.3. Pin Signal Descriptions

3.3.1. Analog Signals

Table 4 Analog Signals

Signal name	Pin type	Description	LQFP80	LQFP64	HTQFP48	VQFN32
A0	I	ADC-A input 0	19	15	11	7
A1	I	ADC-A input 1	18	14	10	7
A2	I	ADC-A input 2	4	2	2	32
A3	I	ADC-A input 3	12	8	5	3
A4	I	ADC-A input 4	27	23	19	12
A5	I	ADC-A input 5	17	13	9	6
A6	I	ADC-A input 6	10	6	4	2
A7	I	ADC-A input 7	23	19	15	8
A8	I	ADC-A input 8	24	20	16	9
A9	I	ADC-A input 9	28	24	20	13
A10	I	ADC-A input 10	29	25	21	13
A11	I	ADC-A input 11	16	12	8	6
A12	I	ADC-A input 12	22	18	14	8
A14	I	ADC-A input 14	15	11	7	5
A15	I	ADC-A input 15	34	28		
AIO225	I	Analog pin for digital input 225	27	23	19	12
AIO231	I	Analog pin for digital input 231	19	15	11	7
AIO232	I	Analog pin for digital input 232	18	14	10	7
AIO233	I	Analog pin for digital input 233	14	10	7	5
AIO237	I	Analog pin for digital input 237	16	12	8	6
AIO238	I	Analog pin for digital input 238	22	18	14	8
AIO239	I	Analog pin for digital input 239	15	11	7	5
AIO241	I	Analog pin for digital input 241	24	20	16	9
AIO244	I	Analog pin for digital input 244	17	13	9	6
AIO245	I	Analog pin for digital input 245	23	19	15	8
C0	I	ADC-C input 0	33	27	22	
C1	I	ADC-C input 1	22	18	14	8
C2	I	ADC-C input 2	17	13	9	6
C3	I	ADC-C input 3	23	19	15	8
C4	I	ADC-C input 4	35	29	23	
C5	I	ADC-C input 5	12	8	5	3
C6	I	ADC-C input 6	11	7	4	2
C7	I	ADC-C input 7	14	10	7	5
C8	I	ADC-C input 8	28	24	20	13
C9	I	ADC-C input 9	13	9	6	4
C10	I	ADC-C input 10	29	25	21	13

Signal name	Pin type	Description	LQFP80	LQFP64	HTQFP48	VQFN32
C11	I	ADC-C input 11	24	20	16	9
C14	I	ADC-C input 14	27	23	19	12
C15	I	ADC-C input 15	36	30	24	
DACA_OUT	O	DAC-A output	19	15	11	7
DACB_OUT	O	DAC-B output	18	14	10	7
VDAC	I	Optional external reference voltage for the on-chip digital-to-analog converters. A 100pF capacitor is connected from this pin to VSSA whether the pin is used as an ADC input or a DAC reference. This capacitor cannot be disabled. If the pin is used as a reference, ensure that no large current flows through it.	17	13	9	6
COMP1_HN0	I	COMP-1 high comparator negative input 0	14	10	7	5
COMP1_HN1	I	COMP-1 high comparator negative input 1	16	12	8	6
COMP1_HP0	I	COMP-1 high comparator positive input 0	13	9	6	4
COMP1_HP1	I	COMP-1 high comparator positive input 1	16	12	8	6
COMP1_HP2	I	COMP-1 high comparator positive input 2	10	6	4	2
COMP1_HP3	I	COMP-1 high comparator positive input 3	14	10	7	5
COMP1_HP4	I	COMP-1 high comparator positive input 4	18	14	10	7
COMP1_LN0	I	COMP-1 low comparator negative input 0	14	10	7	5
COMP1_LN1	I	COMP-1 low comparator negative input 1	16	12	8	6
COMP1_LP0	I	COMP-1 low comparator positive input 0	13	9	6	4
COMP1_LP1	I	COMP-1 low comparator positive input 1	16	12	8	6
COMP1_LP2	I	COMP-1 low comparator positive input 2	10	6	4	2
COMP1_LP3	I	COMP-1 low comparator positive input 3	14	10	7	5
COMP1_LP	I	COMP-1 low comparator positive	18	14	10	7

Signal name	Pin type	Description	LQFP80	LQFP64	HTQFP48	VQFN32
4		input 4				
COMP2_HN0	I	COMP-2 high comparator negative input 0	29	25	21	13
COMP2_HN1	I	COMP-2 high comparator negative input 1	22	18	14	8
COMP2_HP0	I	COMP-2 high comparator positive input 0	27	23	19	12
COMP2_HP1	I	COMP-2 high comparator positive input 1	22	18	14	8
COMP2_HP2	I	COMP-2 high comparator positive input 2	28	24	20	13
COMP2_HP3	I	COMP-2 high comparator positive input 3	29	25	21	13
COMP2_HP4	I	COMP-2 high comparator positive input 4	24	20	16	9
COMP2_LN0	I	COMP-2 low comparator negative input 0	29	25	21	13
COMP2_LN1	I	COMP-2 low comparator negative input 1	22	18	14	8
COMP2_LP0	I	COMP-2 low comparator positive input 0	27	23	19	12
COMP2_LP1	I	COMP-2 low comparator positive input 1	22	18	14	8
COMP2_LP2	I	COMP-2 low comparator positive input 2	28	24	20	13
COMP2_LP3	I	COMP-2 low comparator positive input 3	29	25	21	13
COMP2_LP4	I	COMP-2 low comparator positive input 4	24	20	16	9
COMP3_HN0	I	COMP-3 high comparator negative input 0	12	8	5	3
COMP3_HN1	I	COMP-3 high comparator negative input 1	17	13	9	6
COMP3_HP0	I	COMP-3 high comparator positive input 0	11	7	4	2
COMP3_HP1	I	COMP-3 high comparator positive input 1	17	13	9	6
COMP3_HP2	I	COMP-3 high comparator positive input 2	19	15	11	7
COMP3_HP3	I	COMP-3 high comparator positive input 3	12	8	5	3

Signal name	Pin type	Description	LQFP80	LQFP64	HTQFP48	VQFN32
COMP3_HP4	I	COMP-3 high comparator positive input 4	15	11	7	5
COMP3_LN0	I	COMP-3 low comparator negative input 0	12	8	5	3
COMP3_LN1	I	COMP-3 low comparator negative input 1	17	13	9	6
COMP3_LP0	I	COMP-3 low comparator positive input 0	11	7	4	2
COMP3_LP1	I	COMP-3 low comparator positive input 1	17	13	9	6
COMP3_LP2	I	COMP-3 low comparator positive input 2	19	15	11	7
COMP3_LP3	I	COMP-3 low comparator positive input 3	12	8	5	3
COMP3_LP4	I	COMP-3 low comparator positive input 4	15	11	7	5
COMP4_HN0	I	COMP-4 high comparator negative input 0	27	23	19	12
COMP4_HN1	I	COMP-4 high comparator negative input 1	23	19	15	8
COMP4_HP0	I	COMP-4 high comparator positive input 0	28	24	20	13
COMP4_HP1	I	COMP-4 high comparator positive input 1	23	19	15	8
COMP4_HP2	I	COMP-4 high comparator positive input 2	22	18	14	8
COMP4_HP3	I	COMP-4 high comparator positive input 3	27	23	19	12
COMP4_HP4	I	COMP-4 high comparator positive input 4	24	20	16	9
COMP4_LN0	I	COMP-4 low comparator negative input 0	27	23	19	12
COMP4_LN1	I	COMP-4 low comparator negative input 1	23	19	15	8
COMP4_LP0	I	COMP-4 low comparator positive input 0	28	24	20	13
COMP4_LP1	I	COMP-4 low comparator positive input 1	23	19	15	8
COMP4_LP2	I	COMP-4 low comparator positive input 2	22	18	14	8
COMP4_LP3	I	COMP-4 low comparator positive input 3	27	23	19	12

Signal name	Pin type	Description	LQFP80	LQFP64	HTQFP48	VQFN32
COMP4_LP4	I	COMP-4 low comparator positive input 4	24	20	16	9
VREFHI	I	ADC high reference voltage. In external reference mode, drive the high reference voltage onto this pin externally. In internal reference mode, the device drives this pin. In either mode, place a capacitor of at least 2.2μF between VREFHI and VREFLO, as close to the device as possible. On the VQFN32 package, VREFHI is internally connected to VDDA.	20	16	12	
VREFLO	I	ADC low reference voltage	21	17	13	

3.3.2. Digital Signals

Table 5 Digital Signals

Signal name	Pin type	Description	GPIO	LQFP80	LQFP64	HTQFP48	VQFN32
ADCSOCAO	O	ADC start-of-conversion A for an external ADC	8/33/228	10/38/58	6/32/47	4/25	2
ADCSOCBO	O	ADC start-of-conversion B for an external ADC	10/32	49/76	40/63	32	20
CANA_RX	I	CAN-A receive	0/3/5/11/12/18/21/30/33/35/49/230/242	1/12/29/32/34/36/37/38/48/50/60/63/74	8/25/28/30/31/32/39/41/49/52/61	5/21/24/25/31/33/39/42/47	3/13/14/19/21/26/28/30
CANA_TX	O	CAN-A transmit	2/4/7/13/17/19/20/31/32/37/48/224/228	2/10/13/31/33/35/40/46/49/51/59/61/68	6/9/27/29/34/37/40/42/48/50/57	4/6/22/23/29/32/34/38/40/43	2/4/17/20/22/29
PWM1_A	O	PWM-1 output A	0/4/30/224	1/13/59/63	9/48/52	6/38/42	4/28
PWM1_B	O	PWM-1 output B	1/5/31/226	2/11/62/74	7/51/61	4/41/47	2/27/30
PWM2_A	O	PWM-2 output A	2/6/7/41/230	29/61/66/68/80	25/50/55/57/64	21/40/43/48	13/29
PWM2_B	O	PWM-2 output B	3/7/40/227/228	10/28/60/64/68	6/24/49/53/57	4/20/39/43	2/13/26/29
PWM3_A	O	PWM-3 output A	0/4/14/227	28/59/63/79	24/48/52	20/38/42	13/28
PWM3_B	O	PWM-3 output B	1/5/15/230	29/62/74/78	25/51/61	21/41/47	13/27/30

Signal name	Pin type	Description	GPIO	LQFP80	LQFP64	HTQFP48	VQFN32
PWM4_A	O	PWM-4 output A	2/6/22/24/242	12/41/61/67/80	8/35/50/56/64	5/27/40/48	3/15
PWM4_B	O	PWM-4 output B	3/7/23/32	49/60/65/68	40/49/54/57	32/39/43	20/26/29
PWM5_A	O	PWM-5 output A	8/16/37	39/46/58	33/37/47	26/29	17
PWM5_B	O	PWM-5 output B	9/17/35	40/48/75	34/39/62	31	19
PWM6_A	O	PWM-6 output A	10/17/18/226	11/40/50/76	7/34/41/63	4/33	2/21
PWM6_B	O	PWM-6 output B	11/19	37/51	31/42	34	14/22
PWM7_A	O	PWM-7 output A	12/28/41	4/36/66	2/30/55	2/24	32
PWM7_B	O	PWM-7 output B	13/29	3/35	1/29	1/23	31
QEP1_A	I	QEP-1 input A	6/10/20/25/28/35/40/44/224	4/13/33/42/48/64/69/76/80	2/9/27/39/53/63/64	2/6/22/31/44/48	4/19/32
QEP1_B	I	QEP-1 input B	7/11/21/29/37/41/228	3/10/34/37/46/66/68	1/6/28/31/37/55/57	1/4/29/43	2/14/17/29/31
QEP1_INDEX	I/O	QEP-1 index	0/9/13/17/23/31/32/43/ 242	2/12/35/40/49/54/63/65/75	8/29/34/40/52/54/62	5/23/32/42	3/20/28
QEP1_STROBE	I/O	QEP-1 strobe	1/8/12/16/22/30/42/226	1/11/36/39/57/58/62/67	7/30/33/47/51/56	4/24/26/41	2/27
ERRORSTS	O	Error status output. This signal requires an external pull-down resistor.	24/28/29	3/4/41	1/2/35	1/2/27	15/31/32
ExtR	I	External resistor for the internal oscillator. This can improve clock accuracy.	19	51	42	34	22
GPIO0	I/O	General-purpose input/output 0	0	63	52	42	28
GPIO1	I/O	General-purpose input/output 1	1	62	51	41	27
GPIO2	I/O	General-purpose input/output 2	2	61	50	40	
GPIO3	I/O	General-purpose input/output 3	3	60	49	39	26
GPIO4	I/O	General-purpose input/output 4	4	59	48	38	
GPIO5	I/O	General-purpose input/output 5	5	74	61	47	30
GPIO6	I/O	General-purpose input/output 6	6	80	64	48	
GPIO7	I/O	General-purpose input/output 7	7	68	57	43	29

Signal name	Pin type	Description	GPIO	LQFP80	LQFP64	HTQFP48	VQFN32
GPIO8	I/O	General-purpose input/output 8	8	58	47		
GPIO9	I/O	General-purpose input/output 9	9	75	62		
GPIO10	I/O	General-purpose input/output 10	10	76	63		
GPIO11	I/O	General-purpose input/output 11	11	37	31		14
GPIO12	I/O	General-purpose input/output 12	12	36	30	24	
GPIO13	I/O	General-purpose input/output 13	13	35	29	23	
GPIO14	I/O	General-purpose input/output 14	14	79			
GPIO15	I/O	General-purpose input/output 15	15	78			
GPIO16	I/O	General-purpose input/output 16	16	39	33	26	
GPIO17	I/O	General-purpose input/output 17	17	40	34		
GPIO18	I/O	General-purpose input/output 18	18	50	41	33	21
GPIO19	I/O	General-purpose input/output 19	19	51	42	34	22
GPIO20	I/O	General-purpose input/output 20	20	33	27	22	
GPIO21	I/O	General-purpose input/output 21	21	34	28		
GPIO22	I/O	General-purpose input/output 22	22	67	56		
GPIO23	I/O	General-purpose input/output 23	23	65	54		
GPIO24	I/O	General-purpose input/output 24	24	41	35	27	15
GPIO25	I/O	General-purpose input/output 25	25	42			
GPIO26	I/O	General-purpose input/output 26	26	43			
GPIO27	I/O	General-purpose input/output 27	27	44			
GPIO28	I/O	General-purpose input/output 28	28	4	2	2	32

Signal name	Pin type	Description	GPIO	LQFP80	LQFP64	HTQFP48	VQFN32
GPIO29	I/O	General-purpose input/output 29	29	3	1	1	31
GPIO30	I/O	General-purpose input/output 30	30	1			
GPIO31	I/O	General-purpose input/output 31	31	2			
GPIO32	I/O	General-purpose input/output 32	32	49	40	32	20
GPIO33	I/O	General-purpose input/output 33	33	38	32	25	
GPIO34	I/O	General-purpose input/output 34	34	77			
GPIO35	I/O	General-purpose input/output 35	35	48	39	31	19
GPIO37	I/O	General-purpose input/output 37	37	46	37	29	17
GPIO40	I/O	General-purpose input/output 40	40	64	53		
GPIO41	I/O	General-purpose input/output 41	41	66	55		
GPIO42	I/O	General-purpose input/output 42	42	57			
GPIO43	I/O	General-purpose input/output 43	43	54			
GPIO44	I/O	General-purpose input/output 44	44	69		44	
GPIO45	I/O	General-purpose input/output 45	45	73			
GPIO46	I/O	General-purpose input/output 46	46	6			
GPIO48	I/O	General-purpose input/output 48	48	31			
GPIO49	I/O	General-purpose input/output 49	49	32			
GPIO224	I/O	General-purpose input/output 224	224	13	9	6	4
GPIO226	I/O	General-purpose input/output 226	226	11	7	4	2
GPIO227	I/O	General-purpose input/output 227	227	28	24	20	13
GPIO228	I/O	General-purpose input/output 228	228	10	6	4	2

Signal name	Pin type	Description	GPIO	LQFP80	LQFP64	HTQFP48	VQFN32
GPIO230	I/O	General-purpose input/output 230	230	29	25	21	13
GPIO242	I/O	General-purpose input/output 242	242	12	8	5	3
I2CA_SCL	I/OD	I2C-A open-drain bidirectional clock	1/4/8/18/20/27/33/37/43	33/38/44/46/50/54/58/59/62	27/32/37/41/47/48/51	22/25/29/33/38/41	17/21/27
I2CA_SDA	I/OD	I2C-A open-drain bidirectional data	0/5/10/19/21/26/32/35/42/230	29/34/43/48/49/51/57/63/74/76	25/28/39/40/42/52/61/63	21/31/32/34/42/47	13/19/20/22/28/30
I2CB_SCL	I/OD	I2C-B open-drain bidirectional clock	3/9/15/29/227	3/28/60/75/78	1/24/49/62	1/20/39	13/26/31
I2CB_SDA	I/OD	I2C-B open-drain bidirectional data	2/14/28/34/230	4/29/61/77/79	2/25/50	2/21/40	13/32
LINA_RX	I	LIN-A receive	23/29/33/35/42/49/226	3/11/32/38/48/57/65	1/7/32/39/54	1/4/25/31	2/19/31
LINA_TX	O	LIN-A transmit	22/28/32/37/46	4/6/46/49/67	2/37/40/56	2/29/32	17/20/32
CANFDA_RX	I	CAN/CANFD-A receive	0/5/12/21/30/49	1/32/34/36/63/74	28/30/52/61	24/42/47	28/30
CANFDA_TX	O	CAN/CANFD-A transmit	1/4/13/20/31/46/48	2/6/31/33/35/59/62	27/29/48/51	22/23/38/41	27
OUTPUTXBAR1	O	Output X-BAR output 1	2/24/34/227	28/41/61/77	24/35/50	20/27/40	13/15
OUTPUTXBAR2	O	Output X-BAR output 2	3/25/37/242	12/42/46/60	8/37/49	5/29/39	3/17/26
OUTPUTXBAR3	O	Output X-BAR output 3	4/5/14/26/48/224	13/31/43/59/74/79	9/48/61	6/38/47	4/30
OUTPUTXBAR4	O	Output X-BAR output 4	6/15/27/33/49	32/38/44/78/80	32/64	25/48	
OUTPUTXBAR5	O	Output X-BAR output 5	7/28/42	4/57/68	2/57	2/43	29/32
OUTPUTXBAR6	O	Output X-BAR output 6	9/29/43	3/54/75	1/62	1	31
OUTPUTXBAR7	O	Output X-BAR output 7	0/11/16/30/44	1/37/39/63/69	31/33/52	26/42/44	14/28
OUTPUTXBAR8	O	Output X-BAR output 8	17/31/45	2/40/73	34		
PMBUSA_ALERT	I/OD	PMBUS-A open-drain bidirectional alert signal	13/19/27/37/43/45	35/44/46/51/54/73	29/37/42	23/29/34	17/22
PMBUSA_CTL	I/O	PMBUS-A control signal - slave input/master output	12/18/26/35/42/44	36/43/48/50/57/69	30/39/41	24/31/33/44	19/21

Signal name	Pin type	Description	GPIO	LQFP80	LQFP64	HTQFP48	VQFN32
PMBUSA_SCL	I/OD	PMBUS-A open-drain bidirectional clock	3/15/16/24/35/41/230	29/39/41/48/60/66/78	25/33/35/39/49/55	21/26/27/31/39	13/15/19/26
PMBUSA_SDA	I/OD	PMBUS-A open-drain bidirectional data	2/14/17/25/32/34/40/44/46/48	6/31/40/42/49/61/64/69/77/79	34/40/50/53	32/40/44	20
UARTA_RX	I	UART-A receive data	0/3/5/9/17/25/28/35/49	4/32/40/42/48/60/63/74/75	2/34/39/49/52/61/62	2/31/39/42/47	19/26/28/30/32
UARTA_TX	O	UART-A transmit data	1/2/7/8/16/24/29/37/48	3/31/39/41/46/58/61/62/68	1/33/35/37/47/50/51/57	1/26/27/29/40/41/43	15/17/27/29/31
UARTB_RX	I	UART-B receive data	11/13/15/19/23/41	35/37/51/65/66/78	29/31/42/54/55	23/34	14/22
UARTB_TX	O	UART-B transmit data	9/10/12/14/18/22/40	36/50/64/67/75/76/79	30/41/53/56/62/63	24/33	21
UARTC_RX	I	UART-C receive data	21/42/226	11/34/57	7/28	4	2
UARTC_TX	O	UART-C transmit data	20/43/224	13/33/54	9/27	6/22	4
SPIA_CLK	I/O	SPI-A clock	3/9/12/18/28/32/226	4/11/36/49/50/60/75	2/7/30/40/41/49/62	2/4/24/32/33/39	2/20/21/26/32
SPIA_SIMO	I/O	SPI-A slave input, master output (SIMO)	2/7/8/11/16/20/24/224	13/33/37/39/41/58/61/68	9/27/31/33/35/47/50/57	6/22/26/27/40/43	4/14/15/29
SPIA_SOMI	I/O	SPI-A slave output, master input (SOMI)	1/4/10/13/17/21/35/228	10/34/35/40/48/59/62/76	6/28/29/34/39/48/51/63	4/23/31/38/41	2/19/27
SPIA_STE	I/O	SPI-A slave transmit enable (STE)	0/5/11/19/24/29/37/242	3/12/37/41/46/51/63/74	1/8/31/35/37/42/52/61	1/5/27/29/34/42/47	3/14/15/17/22/28/30/31
SYNCOUT	O	External PWM synchronization pulse	6	80	64	48	
TDI	I	JTAG test data input (TDI). TDI is the default mux selection for this pin. The internal pull-up resistor is disabled by default. When using this pin as JTAG TDI, enable the internal pull-up or add an external pull-up resistor on the board to prevent a floating input.	35	48	39	31	19

Signal name	Pin type	Description	GPIO	LQFP80	LQFP64	HTQFP48	VQFN32
TDO	O	JTAG test data output (TDO). TDO is the default mux selection for this pin. The internal pull-up resistor is disabled by default. When JTAG is inactive, TDO is in the high-impedance state and the pin floats. Enable the internal pull-up or add an external pull-up resistor on the board to prevent a floating GPIO input.	37	46	37	29	17
X1	I/O	Crystal oscillator or single-ended clock input. Device initialization software must configure this pin before enabling the crystal oscillator. To use this oscillator, connect a quartz crystal circuit to X1 and X2. This pin can also accept a single-ended 3.3V clock.	19	51	42	34	22
X2	I/O	Crystal oscillator output.	18	50	41	33	21
XCLKOUT	O	External clock output. This pin outputs a divided version of the selected clock signal from the device.	16/18	39/50	33/41	26/33	21

3.3.3. Power Supply and Grounding

Table 6 Power Supply and Grounding

Signal name	Pin type	Description	LQFP80	LQFP64	HTQFP48	VQFN32
VDD		1.1V digital logic supply pin. See the Power Management Module (PMM) section for usage details.	8/53/71	4/44/59	36/45	24
VDDA		3.3V analog supply pin. Place a decoupling capacitor of at least 2.2μF on each pin. On the VQFN32 package, VREFHI is internally connected to VDDA. See the Power Management Module (PMM) section for usage details.	26	22	18	11
VDDIO		3.3V digital I/O supply pin. See the Power Management Module (PMM) section for usage details.	7/52/72	43/60	35/46	23
VREGENZ	I	Internal voltage regulator enable with an internal pull-down resistor. Connect low to VSS to enable the internal VREG. Connect high to VDDIO to use an external supply.	56	46	37	25
VSS		Digital ground. For VQFN packages, solder the ground pad on the bottom of the package to the PCB ground plane.	9/30/55/70	5/26/45/58	PAD	PAD
VSSA		Analog ground	25	21	17	10

3.3.4. Debug and Reset

Table 7 Debug and Reset

Signal name	Pin type	Description	LQFP80	LQFP64	HTQFP48	VQFN32
TCK(SWCLK)	I	JTAG test clock with an internal pull-up resistor. In SWD debug mode, this pin serves as the SWD clock (SWCLK).	45	36	28	16
TMS(SWDIO)	I/O	JTAG test mode select with an internal pull-up resistor. In SWD debug mode, this pin serves as the SWD serial data line (SWDIO).	47	38	30	18
TDI	I	JTAG test data input (TDI). The internal pull-up is disabled by default. When using this pin as JTAG TDI, enable the internal pull-up or add an external pull-up resistor to prevent a floating input.	48	39	31	19
TDO	O	JTAG test data output (TDO).The internal pull-up is disabled by default. When JTAG is inactive, TDO is in the high-impedance state and the pin floats. Enable the internal pull-up or add an external pull-up resistor to prevent a floating GPIO input.	46	37	29	17

Signal name	Pin type	Description	LQFP80	LQFP64	HTQFP48	VQFN32
XRSn	I/OD	Device reset(input) andwatchdogreset (output). The device drives this pin low at power-up. External circuitry can also drive this pin to reset the device. The MCU also drives it low during awatchdog reset. During watchdog reset, XRSn isheld low for the watchdog reset duration of810OSCCLK cycles. Place a 2.2kΩ to 10kΩ resistor betweenXRSn and VDDIO. If a noise-filtering capacitor is connected between XRSn and VSS, its capacitance must be 100nF or less. These values allow the watchdog to drive XRSn correctly toVOLwithin 810 OSCCLK cycles when watchdog reset is asserted. This pin is an open-drain output with an internal pull-up. Use an open-drain device if the pin is driven externally.	5	3	3	1

3.4. Pin Multiplexing

3.4.1. GPIO Multiplexing Pins

Table 8 GPIO Multiplexing Pins

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO0	PWM1_A	CANA_RX	OUTPUTXBAR7	UARTA_RX	I2CA_SDA	SPIA_STE		CANFDA_RX		QEP1_INDEX		PWM3_A	
GPIO1	PWM1_B			UARTA_TX	I2CA_SCL	SPIA_SOMI	QEP1_STROBE	CANFDA_TX				PWM3_B	
GPIO2	PWM2_A			OUTPUTXBAR1	PMBUSA_SDA	SPIA_SIMO	UARTA_TX		I2CB_SDA		CANA_TX	PWM4_A	
GPIO3	PWM2_B	OUTPUTXBAR2		OUTPUTXBAR2	PMBUSA_SCL	SPIA_CLK	UARTA_RX		I2CB_SCL		CANA_RX	PWM4_B	
GPIO4	PWM3_A	I2CA_SCL	CANFDA_TX	OUTPUTXBAR3	CANA_TX						SPIA_SOMI	PWM1_A	
GPIO5	PWM3_B	I2CA_SDA	OUTPUTXBAR3	CANFDA_RX	CANA_RX	SPIA_STE			UARTA_RX			PWM1_B	
GPIO6	PWM4_A	OUTPUTXBAR4	SYNCOUT	QEP1_A								PWM2_A	
GPIO7	PWM4_B	PWM2_A	OUTPUTXBAR5	QEP1_B		SPIA_SIMO			UARTA_TX		CANA_TX	PWM2_B	
GPIO8	PWM5_A		ADCSOCAO	QEP1_STROBE	UARTA_TX	SPIA_SIMO	I2CA_SCL						
GPIO9	PWM5_B	UARTB_TX	OUTPUTXBAR6	QEP1_INDEX	UARTA_RX	SPIA_CLK					I2CB_SCL		
GPIO10	PWM6_		ADCSOC	QEP1_A	UARTB_T	SPIA_SOMI	I2CA_SDA						

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
	A		BO		X								
GPIO11	PWM6_B	CANA_RX	OUTPUTXBAR7	QEP1_B	UARTB_RX	SPIA_STE				SPIA_SIMO			
GPIO12	PWM7_A		CANFDA_RX	QEP1_STROBE	UARTB_TX	PMBUSA_CTL			SPIA_CLK	CANA_RX		TRACED2	
GPIO13	PWM7_B		CANFDA_TX	QEP1_INDEX	UARTB_RX	PMBUSA_ALERT			SPIA_SOMI	CANA_TX		TRACED3	
GPIO14		UARTB_TX		I2CB_SDA	OUTPUTXBAR3	PMBUSA_SDA				PWM3_A			
GPIO15		UARTB_RX		I2CB_SCL	OUTPUTXBAR4	PMBUSA_SCL				PWM3_B			
GPIO16	SPIA_SIMO		OUTPUTXBAR7	PWM5_A	UARTA_TX		QEP1_STROBE	PMBUSA_SCL	XCLKOUT			TRACED0	
GPIO17	SPIA_SOMI		OUTPUTXBAR8	PWM5_B	UARTA_RX		QEP1_INDEX	PMBUSA_SDA	CANA_TX		PWM6_A	TRGIO	
GPIO18	SPIA_CLK	UARTB_TX	CANA_RX	PWM6_A	I2CA_SCL			PMBUSA_CTL	XCLKOUT				X2
GPIO19	SPIA_STE	UARTB_RX	CANA_TX	PWM6_B	I2CA_SDA			PMBUSA_ALERT					X1
GPIO20	QEP1_A		CANA_TX		SPIA_SIMO		CANFDA_TX		I2CA_SCL			UARTC_TX	
GPIO21	QEP1_B		CANA_RX		SPIA_SOMI		CANFDA_RX		I2CA_SDA			UARTC_RX	
GPIO22	QEP1_STROBE		UARTB_TX				LINA_TX				PWM4_A		
GPIO23	QEP1_I		UARTB_R				LINA_RX				PWM4_B		

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
	NDEX		X										
GPIO24	OUTPUTXBAR1		SPIA_STE	PWM4_A	SPIA_SIMO			PMBUSA_SCL	UARTA_TX	ERRORSTS			
GPIO25	OUTPUTXBAR2			QEP1_A				PMBUSA_SDA	UARTA_RX				
GPIO26	OUTPUTXBAR3			OUTPUTXBAR3				PMBUSA_CTL	I2CA_SDA				
GPIO27	OUTPUTXBAR4			OUTPUTXBAR4				PMBUSA_ALERT	I2CA_SCL				
GPIO28	UARTA_RX		PWM7_A	OUTPUTXBAR5	QEP1_A			LINA_TX	SPIA_CLK	ERRORSTS	I2CB_SDA	TRACECLK	
GPIO29	UARTA_TX		PWM7_B	OUTPUTXBAR6	QEP1_B			LINA_RX	SPIA_STE	ERRORSTS	I2CB_SCL	TRACED2	
GPIO30	CANA_RX			OUTPUTXBAR7	QEP1_STROBE			CANFDA_RX	PWM1_A			TRACED1	
GPIO31	CANA_TX			OUTPUTXBAR8	QEP1_INDEX			CANFDA_TX	PWM1_B			TRACECLK	
GPIO32	I2CA_SDA	QEP1_INDEX	SPIA_CLK	PWM4_B	LINA_TX			CANA_TX	PMBUSA_SDA	ADCSOCBO		TRGIO	
GPIO33	I2CA_SCL			OUTPUTXBAR4	LINA_RX			CANA_RX		ADCSOCAO		TRACED1	
GPIO34	OUTPUTXBAR1				PMBUSA_SDA						I2CB_SDA	TRACED3	
GPIO35	UARTA_RX	SPIA_SOMI	I2CA_SDA	CANA_RX	PMBUSA_SCL	LINA_RX	QEP1_A	PMBUSA_CTL	PWM5_B			TDI	
GPIO37	OUTPU	SPIA_STE	I2CA_SCL	UARTA_TX	CANA_TX	LINA_TX	QEP1_B	PMBUSA	PWM5_A			TDO	

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
	TXBAR2							_ALERT					
GPIO40				PWM2_B	PMBUSA_SDA		UARTB_TX	QEP1_A					
GPIO41	PWM7_A			PWM2_A	PMBUSA_SCL		UARTB_RX	QEP1_B					
GPIO42		LINA_RX	OUTPUTXBAR5	PMBUSA_CTL	I2CA_SDA	UARTC_RX		QEP1_STROBE					
GPIO43			OUTPUTXBAR6	PMBUSA_ALERT	I2CA_SCL	UARTC_TX	PMBUSA_ALERT	QEP1_INDEX					
GPIO44			OUTPUTXBAR7	QEP1_A	PMBUSA_SDA		PMBUSA_CTL						
GPIO45			OUTPUTXBAR8				PMBUSA_ALERT						
GPIO46			LINA_TX	CANFDA_TX			PMBUSA_SDA						
GPIO48	OUTPUTXBAR3		CANA_TX	CANFDA_TX	UARTA_TX		PMBUSA_SDA						
GPIO49	OUTPUTXBAR4		CANA_RX	CANFDA_RX	UARTA_RX		LINA_RX						
GPIO224				OUTPUTXBAR3	SPIA_SIMO		PWM1_A	CANA_TX	QEP1_A		UARTC_TX		
GPIO226			LINA_RX	PWM6_A	SPIA_CLK		PWM1_B		QEP1_STROBE		UARTC_RX		
GPIO227	I2CB_SCL		PWM3_A	OUTPUTXBAR1	PWM2_B								
GPIO228			ADCSOC	CANA_TX	SPIA_SOM		PWM2_B		QEP1_B				

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
			AO		I								
GPIO230	I2CB_SDA		PWM3_B	CANA_RX	PWM2_A	I2CA_SDA	PMBUSA_SCL						
GPIO242				OUTPUTXBAR2	SPIA_STE		PWM4_A	CANA_RX	QEP1_INDEX				
AIO225													
AIO231													
AIO232													
AIO233													
AIO237													
AIO238													
AIO239													
AIO241													
AIO244													
AIO245													

3.4.2. Analog Input Pins Multiplexed as Digital Inputs (AIO)

Port H GPIOs are multiplexed with analog pins and are also called AIOs. These pins operate only in input mode. By default, they function as analog pins and the GPIOs are in a high-impedance state. The GPHAMSEL register configures digital or analog operation on these pins.

Note: Digital signals with sharp edges (high dv/dt) on AIOs may cause crosstalk on adjacent analog signals. If adjacent channels are used for analog functions, limit the edge rate of signals connected to the AIOs.

3.4.3. Digital Inputs and Outputs on ADC Pins (AGPIO)

Some GPIOs are multiplexed with analog pins and provide digital input and output functions. These are called AGPIOs. Unlike AIOs, AGPIOs have full input and output capability.

AGPIOs are disconnected by default and must be configured. The following table shows the AGPIO configuration. To enable analog functions, configure the AGPIOCTRLx registers in the analog subsystem. To enable digital functions, configure the GPxAMSEL registers described in the General-Purpose Input/Output (GPIO) chapter.

Table 9 AGPIO Configuration

AGPIOCTRLx.GPIOy (Default = 0)	GPxAMSEL.GPIOy (Default = 1)	Pin connected to	
		ADC	GPIOy
0	0	-	Yes
0	1	- (1)	- (1)
1	0	-	Yes
1	1	Yes	-

Note: Digital signals with sharp edges (high dv/dt) on AGPIOs may cause crosstalk on adjacent analog signals. If adjacent channels are used for analog functions, limit the edge rate of signals connected to the AGPIOs.

(1) By default, no signal is connected to an AGPIO pin. Select one of the other rows in the table to enable a pin function.

3.4.4. GPIO Input X-BAR

The Input X-BAR routes GPIO signals to various IP blocks, including ADC, CAP, PWM, and external interrupts (see the following figure). The following table lists the Input X-BAR destinations. Refer to the user manual for Input X-BAR configuration details.

Figure 5 Input X-BAR

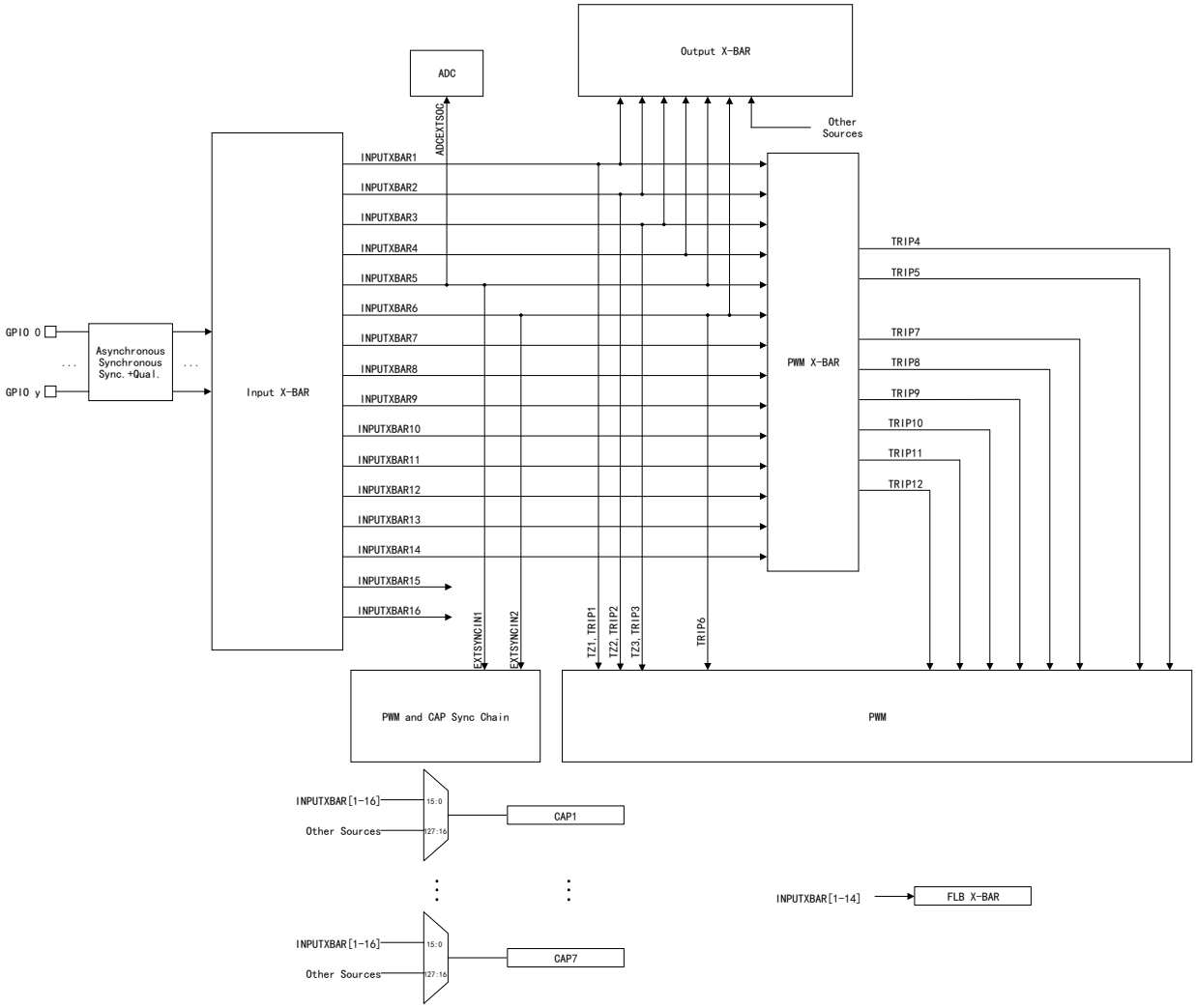


Table 10 Input X-BAR Destinations

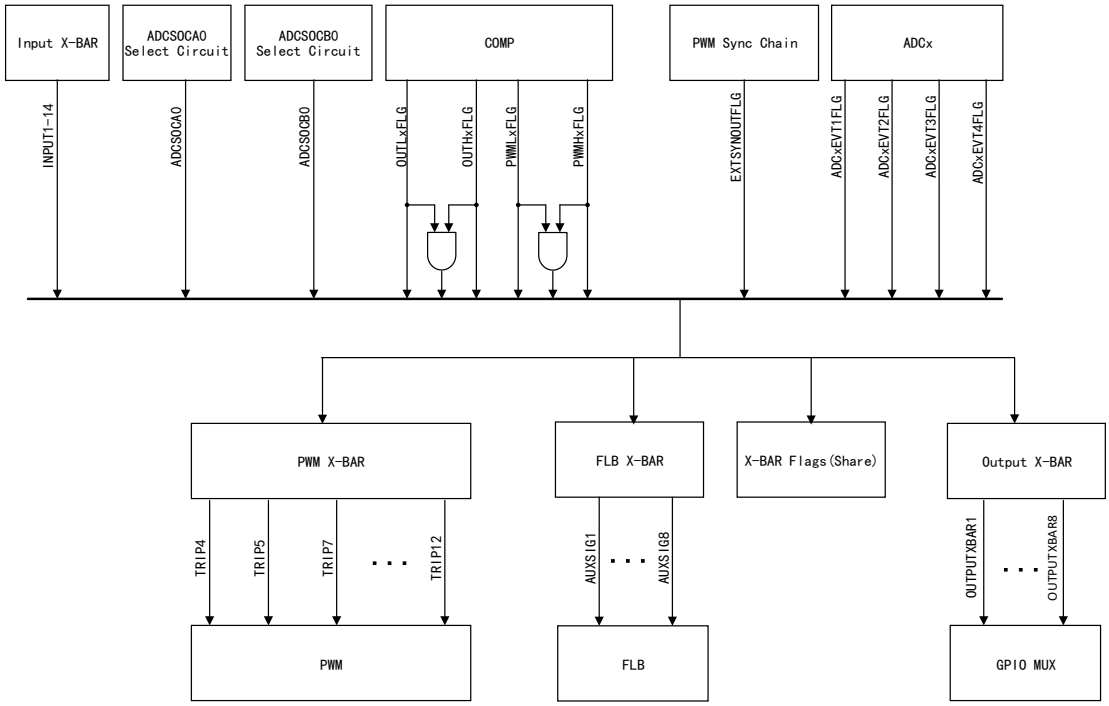
Input	Destination IP block
Input 1	Output X-BAR, PWM X-BAR, CAPx, PWM[TZ1,TRIP1], FLB
Input 2	Output X-BAR, PWM X-BAR, CAPx, PWM[TZ2,TRIP2], FLB
Input 3	Output X-BAR, PWM X-BAR, CAPx, PWM[TZ3,TRIP3], FLB
Input 4	Output X-BAR, PWM X-BAR, CAPx, FLB, CPU
Input 5	Output X-BAR, PWM X-BAR, CAPx, ADCEXTSOC, EXTSYNCIN1, FLB, CPU
Input 6	Output X-BAR, PWM X-BAR, CAPx, PWM[TRIP2], PWM[TRIP6], EXTSYNCIN2, FLB, CPU
Input 7	PWM X-BAR，CAPx，FLB
Input 8	PWM X-BAR，CAPx，FLB
Input 9	PWM X-BAR，CAPx，FLB
Input 10	PWM X-BAR，CAPx，FLB
Input 11	PWM X-BAR，CAPx，FLB

Input	Destination IP block
Input 12	PWM X-BAR，CAPx，FLB
Input 13	PWM X-BAR，CAPx，FLB，CPU
Input 14	PWM X-BAR，CAPx，FLB，CPU
Input 15	CAPx
Input 16	CAPx

3.4.5. GPIO Output X-BAR, PWM X-BAR, and FLB XBAR

The Output X-BAR has eight outputs routed to the GPIO module. The PWM X-BAR has eight outputs routed to each PWM module.

Figure 6 Output X-BAR, PWM X-BAR, and FLB XBAR Sources



3.5. Pins with Internal Pull-up or Pull-down Resistors

Some device pins have internal pull-up or pull-down resistors. The following table lists the pull direction and when it is active. GPIO pull-ups are disabled by default and can be enabled by software. To prevent floating unbonded inputs, the boot ROM enables internal pull-ups on GPIOs that are unbonded in a given package. Pull-ups and pull-downs on the other pins listed in the table are always enabled and cannot be disabled.

Table 11 Pins with Internal Pull-up and Pull-down Resistors

Pin	Reset (XRSn = 0)	Device boot	Applications
GPIOx	Pull-up disabled	Pull-up disabled (1)	Application-defined
GPIO35/TDI	Pull-up disabled		Application-defined

Pin	Reset (XRSn = 0)	Device boot	Applications
GPIO37/TDO	Pull-up disabled		Application-defined
TCK	Pull-up active		
TMS	Pull-up active		
XRSn	Pull-up active		
Other pins (including AIO)	No pull-up or pull-down		

Note:

(1) Internal pull-ups on unbonded pins in a given package are enabled by the boot ROM.

3.6. Connections for Unused Pins

For applications that do not use all device functions, the following table lists acceptable connections for unused pins. When multiple options are listed, any one is acceptable. Connect pins not listed here as described in the Pin Signals section.

Table 12 Connections for Unused Pins

Signal name	Acceptable connection
Analog	
VREFHI	Connect to VDDA (only when the ADC is unused)
VREFLO	Tie to VSSA
Analog input pins	• No connection • Tie to VSSA • Connect to VSSA through a resistor
Analog input pins (shared with GPIO)	• No connection • Connect to VSSA through a resistor
Digital	
GPIOx	• No connection (input mode, internal pull-up enabled) • No connection (output mode, internal pull-up disabled) • Pull-up or pull-down resistor (any resistance, input mode, internal pull-up disabled)
GPIO35/TDI	When the TDI mux option is selected (default), the GPIO is in input mode. • Enable the internal pull-up resistor • External pull-up resistor
GPIO37/TDO	When the TDO mux option is selected (default), the GPIO is in output mode only during JTAG activity; otherwise, it is in the high-impedance state. Bias this pin to prevent additional current in the input buffer. • Enable the internal pull-up resistor • External pull-up resistor
TCK	• No connection • Pull-up resistor

Signal name	Acceptable connection
TMS	Pull-up resistor
GPIO19/X1	Disable XTAL and: • Input mode, internal pull-up enabled • Input mode, external pull-up or pull-down resistor • Output mode, internal pull-up disabled
GPIO18/X2	Disable XTAL and: • Input mode, internal pull-up enabled • Input mode, external pull-up or pull-down resistor • Output mode, internal pull-up disabled
Power Supply and Grounding	
VDD	Connect all VDD pins as described in the Pin Signal Descriptions section. Do not use these pins to bias external circuitry.
VDDA	Connect to VDDIO if a dedicated analog supply is not used.
VDDIO	Connect all VDDIO pins as described in the Pin Signal Descriptions section.
VSS	Connect all VSS pins to board ground.
VSSA	Connect to VSS if a separate analog ground is not used.

4. Module Description

4.1. Introduction

G32R502x is a high-performance MCU developed by Geehy for real-time control applications. It integrates up to one Arm® Cortex® -M52 processor based on the Arm® v8.1-M architecture and is suitable for home appliances, photovoltaic inverters, digital power supplies, and on-board chargers (OBC).

The G32R502x MCU operates at up to 200MHz and implements the Arm® v8.1-M Custom Datapath Extension (CDE). Its innovative Zidian Math Instruction Extension further improves processing performance. Zidian accelerates algorithms containing trigonometric operations commonly used in transforms and torque-loop calculations, and reduces latency in complex mathematical operations common in encoding applications.

G32R502x supports up to 256KB of internal Flash, organized as two independent 128KB banks that support concurrent programming and execution. The built-in CFGSMS efficiently partitions the 40KB on-chip SRAM into 8KB logical blocks that can be configured as ITCM, DTCM, or SRAM. G32R502x also supports Flash and RAM ECC/parity checking and security attribute configuration.

G32R502x integrates high-performance analog units to improve system control performance. Two independent 12-bit ADCs acquire and process multiple analog signals accurately and efficiently, increasing system throughput. Four comparator subsystems continuously monitor input voltage levels through the trip function.

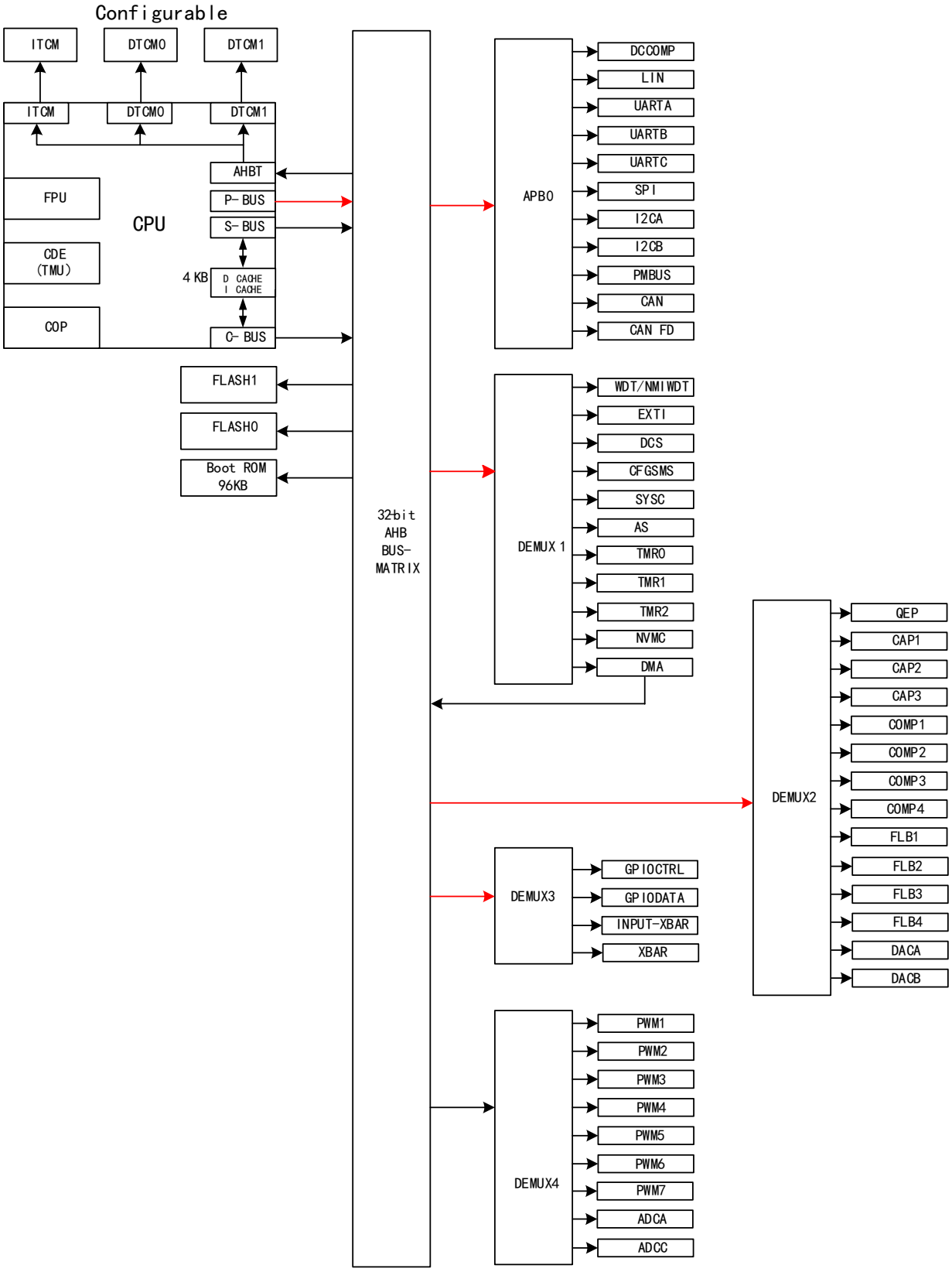
G32R502x includes high-performance control peripherals, with frequency-independent PWM and CAP, for precise system control.

G32R502x integrates general-purpose communication ports, including SPI, UART, I2C, LIN, and CAN/CAN FD, with multiple multiplexing options to meet application communication requirements. It also provides a fully standards-compliant PMBUS interface. JTAG, cJTAG, and SWD interfaces offer debug modes suited to different system environments and performance requirements.

G32R502x supports operating ambient temperatures of -40℃ to 105℃/125℃ and is available in VQFN32, HTQFP48, LQFP64, and LQFP80 packages.

4.2. Functional Block Diagram

Figure 7 Functional Block Diagram



4.3. Memory

4.3.1. Memory Mapping

The memory map is shown in the following table.

Table 13 Memory Mapping

Address range (Hex)	Size (Max)	Description
0x0000_0000 - 0x0000_7FFF	32KB	CPU ITCM (Default 16KB)
0xA000_0000 - 0xA000_7FFF	32KB	CPU ITCM (CPU-AHBT) (Default 16KB)
0x0800_0000 - 0x0803_FFFF	256KB	FLASH memory on BUSMATRIX
0x0810_0000 - 0x0810_BFFF	64KB	FLASH INFO on BUSMATRIX
0x0818_0000 - 0x0818_3FFF	16KB	FLASH INFO1 on BUSMATRIX
0x0900_0000 - 0x0900_7FFF	32KB	FLASH ECC(Main)
0x0902_0000 - 0x0902_1FFF	8KB	FLASH ECC(IFREN)
0x1000_0000 - 0x1001_7FFF	96KB	Boot ROM
0x2000_0000 - 0x2000_7FFF	32KB	CPU DTCM (Default 24KB)
0xA010_0000 - 0xA010_7FFF	32KB	CPU DTCM (CPU-AHBT) (Default 24KB)
0x4000_0000 – 0x4000_FFFF	APB0	APB peripherals
0x4001_0000 – 0x4001_FFFF	DEMUX1	AHB peripherals
0x4002_0000 – 0x4002_FFFF	DEMUX2	AHB peripherals
0x4003_0000 – 0x4003_FFFF	DEMUX3	AHB peripherals
0x5000_0000 – 0x5000_FFFF	DEMUX4	AHB peripherals

4.3.2. Flash Mapping

G32R502x provide up to two Flash banks (128KB each for Bank0/1). Two nonvolatile memory controllers (NVMC) control the Flash banks. The CPU can access FLASH MEM through C-BUS. All Flash erase/write operations are performed through NVMC registers. The FLASH MEM address space is read-only for the CPU and DMA; all writes are ignored. Do not access a Flash bank undergoing erase or programming.

Note: When A/B SWAP is enabled, bank0 and bank1 have the same address.

Table 14 Flash Sector Addresses in Single-bank Configuration (256-bit Read Width)

IP	Name	Sector via C-BUS interface	Sector size	Bank number
Main memory	Sector0	0x0800_0000~0x0800_3FFF	16KByte	Bank0 & Bank1 mix
	Sector1	0x0800_4000~0x0800_7FFF	16KByte	Bank0 & Bank1 mix
	Sector2	0x0800_8000~0x0800_BFFF	16KByte	Bank0 & Bank1 mix

IP	Name	Sector via C-BUS interface	Sector size	Bank number
	…….	…….	…….	Bank0 & Bank1 mix
	Sector14	0x0803_8000~0x0803_BFFF	16KByte	Bank0 & Bank1 mix
	Sector15	0x0803_C000~0x0803_FFFF	16KByte	Bank0 & Bank1 mix
IFREN	Bank0 back-up sector0	0x0810_0000~0x0810_1FFF	8KByte	Bank0
	Bank0 back-up sector1	0x0810_2000~0x0810_3FFF	8KByte	Bank0
	Bank0 back-up sector2	0x0810_4000~0x0810_5FFF	8KByte	Bank0
	Bank0 back-up sector3	0x0810_6000~0x0810_7FFF	8KByte	Bank0
	Bank1 User Option byte	0x0810_8000~0x0810_9FFF	8KByte	Bank1
	Bank1 OTP	0x0810_A000~0x0810_BFFF	8KByte	Bank1
	Bank1 back-up sector2	0x0810_C000~0x0810_DFFF	8KByte	Bank1
	Bank1 back-up sector3	0x0810_E000~0x0810_FFFF	8KByte	Bank1
IFREN1	Bank0 FLASH trimming	0x0818_0000~0x0818_1FFF	8KByte	Bank0
	Bank1 FLASH trimming	0x0818_2000~0x0818_3FFF	8KByte	Bank1
ECC	Main ECC	0x0900_0000~0x0900_7FFF	32Kbyte	Bank0 & Bank1 mix
	Bank0 IFREN ECC	0x0902_0000~0x0902_0FFF	4KByte	Bank0
	Bank1 IFREN ECC	0x0902_1000~0x0902_1FFF	4KByte	Bank1

Table 15 Flash Sector Addresses in Dual-bank Configuration (128-bit Read Width)

IP	Name	Sector via C-BUS interface	Sector size	Bank number
Main memory bank0	Sector0	0x0800_0000~0x0800_1FFF	8KByte	Bank0
	Sector1	0x0800_2000~0x0800_3FFF	8KByte	Bank0
	Sector2	0x0800_4000~0x0800_5FFF	8KByte	Bank0
	…….	…….	…….	Bank0
	Sector14	0x0801_C000~0x0801_DFFF	8KByte	Bank0
	Sector15	0x0801_E000~0x0801_FFFF	8KByte	Bank0
Main memory bank1	Sector16	0x0802_0000~0x0802_1FFF	8KByte	Bank1
	Sector17	0x0802_2000~0x0802_3FFF	8KByte	Bank1
	Sector18	0x0802_4000~0x0802_5FFF	8KByte	Bank1
	…….	…….	…….	Bank1

IP	Name	Sector via C-BUS interface	Sector size	Bank number
	Sector30	0x0803_C000~0x0803_DFFF	8KByte	Bank1
	Sector31	0x0803_E000~0x0803_FFFF	8KByte	Bank1
IFREN	Bank0 back-up sector0	0x0810_0000~0x0810_1FFF	8KByte	Bank0
	Bank0 back-up sector1	0x0810_2000~0x0810_3FFF	8KByte	Bank0
	Bank0 back-up sector2	0x0810_4000~0x0810_5FFF	8KByte	Bank0
	Bank0 back-up sector3	0x0810_6000~0x0810_7FFF	8KByte	Bank0
	Bank1 User Option byte	0x0810_8000~0x0810_9FFF	8KByte	Bank1
	Bank1 OTP	0x0810_A000~0x0810_BFFF	8KByte	Bank1
	Bank1 back-up sector2	0x0810_C000~0x0810_DFFF	8KByte	Bank1
	Bank1 back-up sector3	0x0810_E000~0x0810_FFFF	8KByte	Bank1
IFREN1	Bank0 FLASH trimming	0x0818_0000~0x0818_1FFF	8KByte	Bank0
	Bank1 FLASH trimming	0x0818_2000~0x0818_3FFF	8KByte	Bank1
ECC	Bank0 Main ECC	0x0900_0000~0x0900_3FFF	16KByte	Bank0
	Bank1 Main ECC	0x0900_4000~0x0900_7FFF	16KByte	Bank1
	Bank0 IFREN ECC	0x0902_0000~0x0902_0FFF	4KByte	Bank0
	Bank1 IFREN ECC	0x0902_1000~0x0902_1FFF	4KByte	Bank1

4.3.3. Peripheral Register Memory Map

Table 16 Peripheral Register Memory Map

Bus	IP	Address
APB0	DCCOMP	0x4000_0000-0x4000_03FF
	LIN	0x4000_0400-0x4000_07FF
	UARTA	0x4000_0800-0x4000_0BFF
	UARTB	0x4000_0C00-0x4000_0FFF
	UARTC	0x4000_1000-0x4000_13FF
	SPI	0x4000_1400-0x4000_17FF
	I2CA	0x4000_1800-0x4000_1BFF
	I2CB	0x4000_1C00-0x4000_1FFF
	PMBUS	0x4000_2000-0x4000_23FF

Bus	IP	Address
	CAN	0x4000_2400-0x4000_2BFF
	CANFDA	0x4000_2C00-0x4000_33FF
	CANFDA-SRAM	0x4000_3400-0x4000_43FF
	Reserved	0x4000_4400-0x4000_FFFF
DEMUX1	WDT NMIWDT	0x4001_0000-0x4001_00BF 0x4001_00C0-0x4001_03FF
	EXTI	0x4001_0400-0x4001_07FF
	DCS	0x4001_0800-0x4001_27FF
	CFGSMS	0x4001_2800-0x4001_2BFF
	SYSC	0x4001_2C00-0x4001_6BFF
	AS	0x4001_6C00-0x4001_6FFF
	TMR0	0x4001_7000-0x4001_73FF
	TMR1	0x4001_7400-0x4001_77FF
	TMR2	0x4001_7800-0x4001_7BFF
	NVMC	0x4001_7C00-0x4001_83FF
	DMA	0x4001_8400-0x4001_87FF
	Reserved	0x4001_8800-0x4001_FFFF
DEMUX2	QEP	0x4002_0000-0x4002_03FF
	CAP1	0x4002_0400-0x4002_07FF
	CAP2	0x4002_0800-0x4002_0BFF
	CAP3	0x4002_0C00-0x4002_0FFF
	COMP1	0x4002_1000-0x4002_13FF
	COMP2	0x4002_1400-0x4002_17FF
	COMP3	0x4002_1800-0x4002_1BFF
	COMP4	0x4002_1C00-0x4002_1FFF
	FLB1	0x4002_2000-0x4002_27FF
	FLB2	0x4002_2800-0x4002_FFFF
	FLB3	0x4002_3000-0x4002_37FF
	FLB4	0x4002_3800-0x4002_3FFF
	DACA	0x4002_4000-0x4002_43FF
	DACB	0x4002_4400-0x4002_47FF
	Reserved	0x4002_4800-0x4002_FFFF
DEMUX3	GPIOCTRL	0x4003_0000-0x4003_07FF

Bus	IP	Address
	GPIODATA	0x4003_0800-0x4003_0BFF
	INPUTXBAR	0x4003_0C00-0x4003_0C7F
	SyncSocREG	0x4003_0C80-0x4003_0FFF
	XBAR_REG	0x4003_1000-0x4003_103F
	PWM_XBAR_REG	0x4003_11C0-0x4003_123F
	FLB_XBAR_REG	0x4003_1240-0x4003_12BF
	OUTPUT_XBAR_REG	0x4003_12C0-0x4003_13FF
	Reserved	0x4003_1400-0x4003_FFFF
DEMUX4	PWM1	0x5000_0000-0x5000_03FF
	PWM2	0x5000_0400-0x5000_07FF
	PWM3	0x5000_0800-0x5000_0BFF
	PWM4	0x5000_0C00-0x5000_0FFF
	PWM5	0x5000_1000-0x5000_13FF
	PWM6	0x5000_1400-0x5000_17FF
	PWM7	0x5000_1800-0x5000_1BFF
	ADCA	0x5000_1C00-0x5000_1FFF
	ADCC	0x5000_2000-0x5000_23FF
	Reserved	0x5000_2400-0x5000_FFFF

4.3.4. Memory Types

4.3.4.1. RAM(ITCM/DTCM/SRAM)

G32R502x devices efficiently partition the 40KB on-chip RAM to configure ITCM and DTCM of different sizes. The CPU subsystem has two small, non-secure, tightly coupled memory blocks, ITCM and DTCM, accessible only by the CPU. G32R502x also supports RAM ECC checking.

4.4. Identification

The following table lists device identification registers. Refer to the PARTIDH and PARTIDL register descriptions for identification availability in production devices and other device information.

Table 17 Device Identification Registers

Name	Address	Size (×8)	Description	
PARTIDH	0x4001_3114	4	G32R502 device model identification number	0x01FF 0400
REVID	0x4001_3118	4	Device revision number	0x0000 01F6

Name	Address	Size (×8)	Description	
			Revision 0	
UID_UNIQUE	0x0810 AF88	4	Unique identification number. This number differs for each individual device with the same PARTIDH and can be used as an application serial number.	

4.5. Bus Architecture - Peripheral Connections

Table 18 Bus Master Access to Peripherals

Peripheral	DMA	CPU
CPU timer		Supported
System configuration (WDT, NMIWDT, LPM, peripheral clock gating)		Supported
Device functions and peripheral reset		Supported
Clock and PLL configuration		Supported
Flash configuration		Supported
Reset configuration		Supported
GPIO pin mapping and configuration		Supported
GPIO data		Supported
DMA trigger source selection		Supported
PWM/HRPWM	Supported	Supported
CAP	Supported	Supported
QEP (1)	Supported	Supported
FLB(2)		Supported
Analog system control		Supported
ADC configuration	Supported	Supported
ADC results	Supported	Supported
COMP (1)	Supported	Supported
DAC (1)	Supported	Supported
CAN	Supported	Supported
CAN FD(1)	Supported	Supported
SPI	Supported	Supported
I2C	Supported	Supported
PMBUS	Supported	Supported
UART	Supported	Supported
LIN	Supported	Supported

Note:

(1) These modules are accessible by DMA but cannot trigger DMA transfers.

(2) FLB can trigger DMA transfers but is not accessible by DMA.

4.6. Processor

G32R502x integrates an Arm® Cortex-M52 core. Cortex-M52 is the second-generation embedded processor in Arm China's Star series, based on the latest Arm® v8.1-M architecture. It is the first locally developed automotive-grade embedded processor supporting functional safety design. It provides enhanced AI and digital signal processing, higher compute density and energy efficiency, and optimized functional safety and information security for IoT and automotive devices.

4.6.1. Floating-Point Unit (FPU)

The Cortex-M52 FPU provides scalar half-precision and single-precision floating-point operations. It supports addition, subtraction, multiplication, division, multiply-accumulate, and square root operations, conversions between fixed-point and floating-point formats, and floating-point constant instructions.

The Cortex-M52 provides floating-point computation, including floating-point extensions, compliant with ANSI/IEEE Std 754-2008, the IEEE Standard for Binary Floating-Point Arithmetic.

4.6.2. Zidian Math Instruction Extension - Trigonometric Math Unit (TMU)

The TMU extends Cortex-M52 and FPU functionality by adding instructions and leveraging existing FPU instructions to accelerate common trigonometric functions and the arithmetic operations listed below.

Table 19 Instructions Supported by TMU

Instruction	C equivalent operation	Pipeline cycles
MPY2PIF32 RaH,RbH	a = b * 2π	1
DIV2PIF32 RaH,RbH	a = b / 2π	1
DIVF32 RaH,RbH,RcH	a = b/c	2
SQRTF32 RaH,RbH	a = sqrt(b)	2
SINPUF32 RaH,RbH	a = sin(b*2π)	2
COSPUF32 RaH,RbH	a = cos(b*2π)	2
ATANPUF32 RaH,RbH	a = atan(b)/2π	2
QUADF32 Sd, Sn, Sm	Operation to assist ATANPU2 calculation	1

No changes are made to existing instructions, pipelines, or the memory bus architecture. All TMU instructions use the existing FPU register set.

4.6.3. CRC Engine and Instructions (VCRC)

CRC algorithms provide a simple way to verify data integrity for large data blocks, communication packets, or code sections. Cortex-M52 + VCRC performs 8-bit, 16-bit, and 32-bit CRC operations. The CRC result register contains the current CRC and is updated whenever a CRC instruction executes.

4.6.4. Fast Integer Division Unit (FINTDIV)

The fast integer division (FINTDIV) unit uniquely supports three division types (truncated, modulo, and Euclidean) for 16-bit/16-bit, 32-bit/16-bit, 32-bit/32-bit, and 64-bit/64-bit operands in unsigned or signed format.

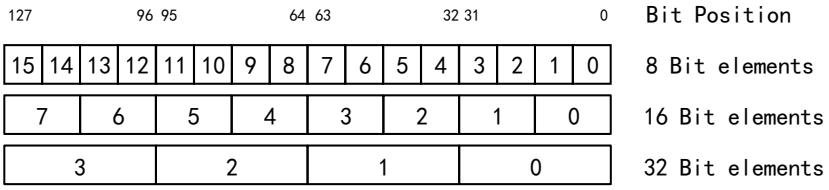
All three division types produce both quotient and remainder and are interruptible.

4.6.5. Helium

Helium™ technology is the M-profile Vector Extension (MVE) for Arm Cortex-M processors. Part of the Arm v8.1-M architecture, it improves performance for DSP and machine learning applications. Helium™ uses single instruction, multiple data (SIMD) to perform the same operation on multiple data elements simultaneously. MVE has integer and floating-point variants; G32R502 implements only the integer variant.

- MVE-I operates on 32-bit, 16-bit, and 8-bit data types, including Q7, Q15, and Q31.
- MVE operations are divided along two orthogonal dimensions: lanes and beats.
- A lane is a portion of a vector register or operation. Data placed in a lane is called an element. Multiple lanes can execute per beat, and each vector instruction has four beats. The supported lane widths and lane operations per beat are:
  - For 64-bit lanes, one beat executes half a lane operation.
  - For 32-bit lanes, one beat executes one lane operation.
  - For 16-bit lanes, one beat executes two lane operations.
  - For 8-bit lanes, one beat executes four lane operations.

Figure 8 Helium Vector Elements



- A beat is one quarter of an MVE vector operation. Since vectors are 128 bits long, one beat of a vector addition produces 32 bits of result data, regardless of lane width. For example, with 8-bit lanes, one beat performs four 8-bit additions. Beats per clock describe how much architectural state is typically updated per architectural clock. Systems are classified as follows:
  - In a single-beat system, one beat can occur per clock.
  - In a dual-beat system, two beats can occur per clock.
  - In a quad-beat system, four beats can occur per clock.

Cortex-M52 implements a single-beat system. Refer to the Cortex-M52 processor documentation for more information.

4.7. Direct Memory Access (DMA)

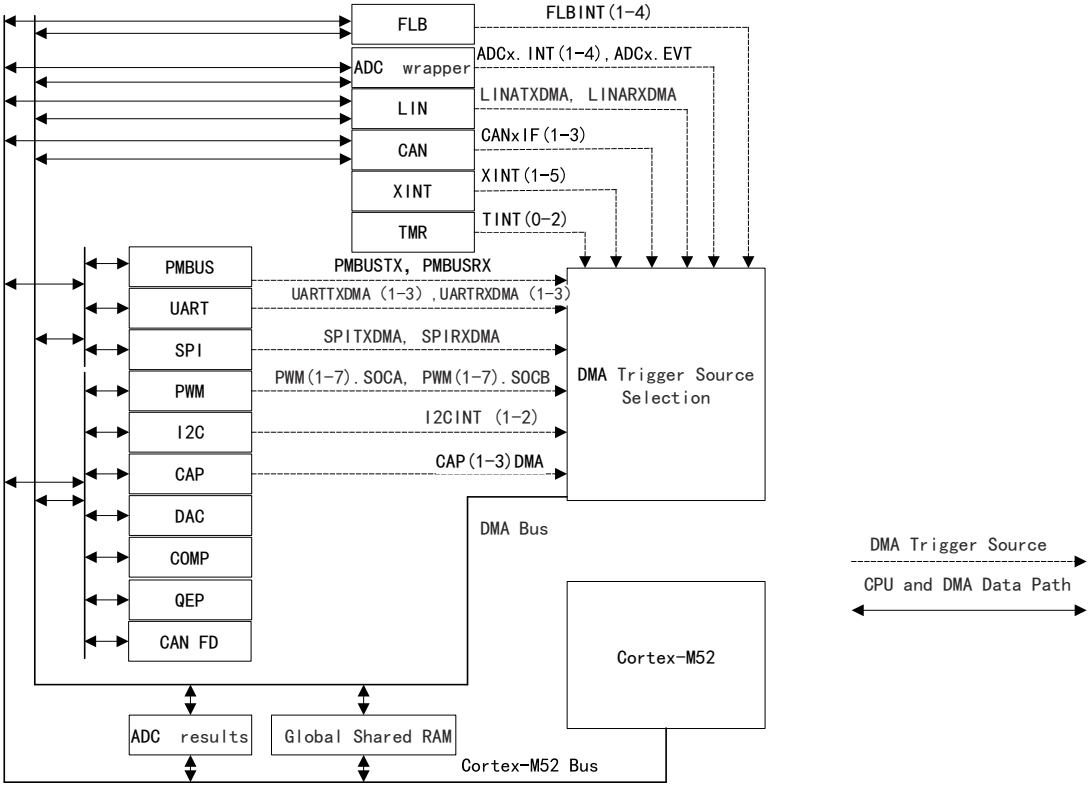
The DMA module transfers data between peripherals and/or memory without CPU intervention,

freeing bandwidth for other system functions. DMA can also reorder data orthogonally during transfers and perform ping-pong operations between buffers. These features help organize data into blocks for optimal CPU processing.

DMA features include:

- Six channels with independent interrupts
- Peripheral interrupt trigger sources
  - ADC interrupt and EVT signals
  - External interrupts
  - PWM SOC signals
  - CPU timers
  - CAP
  - FLB
  - UART transmit and receive
  - SPI transmit and receive
  - I2C transmit and receive
  - CAN transmit and receive
  - LIN transmit and receive
  - PMBUS transmit and receive
- Data sources and destinations:
  - SRAM
  - FLASH
  - ADC result registers
  - Control peripheral registers (PWM, QEP, CAP)
  - DAC
  - COMP
  - SPI, LIN, CAN, CAN FD, UART, I2C, and PMBUS registers
- Word size: 16 or 32 bits (SPI limited to 16 bits)

Figure 9 DMA Block Diagram



DMA Arbitration Logic

DMA data transfers run independently of the CPU. When DMA and the CPU access an address simultaneously, arbitration resolves the conflict. DMA has higher priority than the CPU when accessing any slave (DMA > CPU). If DMA performs a write while the CPU performs a read-write-read operation, the DMA write data is lost. Therefore, avoid CPU and DMA writes in the same cycle.

Table 20 Channel Trigger Source Configuration

Selection value (8-bit)	Channel trigger source
0	No Peripheral
1	ADCA.1
2	ADCA.2
3	ADCA.3
4	ADCA.4
5	ADCAEVT
6-10	No Peripheral
11	ADCC.1
12	ADCC.2
13	ADCC.3
14	ADCC.4
15	ADCCEVT

Selection value (8-bit)	Channel trigger source
16-28	No Peripheral
29	XINT1
30	XINT2
31	XINT3
32	XINT4
33	XINT5
34-35	No Peripheral
36	PWM1.SOCA
37	PWM1.SOCB
38	PWM2.SOCA
39	PWM2.SOCB
40	PWM3.SOCA
41	PWM3.SOCB
42	PWM4.SOCA
43	PWM4.SOCB
44	PWM5.SOCA
45	PWM5.SOCB
46	PWM6.SOCA
47	PWM6.SOCB
48	PWM7.SOCA
49	PWM7.SOCB
50-67	No Peripheral
68	TINT0
69	TINT1
70	TINT2
71-74	No Peripheral
75	CAP1DMA
76	CAP2DMA
77	CAP3DMA
78	PMBUSTX
79	PMBUSRX
80-95	No Peripheral
96	UARTATX
97	UARTARX
98	UARTBTX
99	UARTBRX
100-108	No Peripheral
109	SPIATX
110	SPIARX
111	UARTCTX
112	UARTCRX

Selection value (8-bit)	Channel trigger source
113-116	No Peripheral
117	LINATX
118	LINARX
119-122	No Peripheral
123	I2CATX
124	No Peripheral
125	I2CARX
126	No Peripheral
127	FLB1INT
128	FLB2INT
129	FLB3INT
130	FLB4INT
131-166	No Peripheral
167	CANAIF1
168	CANAIF2
169	CANAIF3
170	I2CBRX
171	I2CBTX
173-179	No Peripheral
180	No Peripheral
181	No Peripheral
182	No Peripheral
183	No Peripheral
184-255	No Peripheral

4.8. ROM

4.8.1. Boot ROM and Peripheral Boot

The device boot ROM contains bootloader software. An internal bootloader programmed by Geehy executes at power-up and after every reset. It acts as the initial program, loading an application into device RAM through any boot-capable peripheral or starting an application in Flash, if configured and available.

Table 21 Default Device Boot Modes

Boot mode	GPIO24 (default boot mode select pin 1)	GPIO32 (default boot mode select pin 0)
UART/wait boot	0	1
CAN	1	0
Flash	1	1

The following table lists boot modes that may be supported by the device. Default boot mode pins are GPIO24 (boot mode pin 1) and GPIO32 (boot mode pin 0). If peripherals also use these pins, weak pull-ups may be selected for the boot mode pins so that peripheral signals can override them. Customers can change the factory-default boot mode pins by programming the user-configurable dual-code security module (DCS) OTP locations.

Table 22 All Available Boot Modes

Boot mode number	Boot mode
1	UART/wait boot
2	CAN
3	Flash
4	Wait
5	RAM
6	SPI master
7	I2C master
10	CAN FD

Note: All supported peripheral boot modes use the first instance of the peripheral (UART, SPI, I2C, CAN, CAN FD, etc.). For example, UART boot uses UARTA. The same rule applies to other peripheral boot modes.

4.8.1.1. Configuring Alternate Boot Mode Select Pins

Users can customize the boot mode select pins by programming BOOTPIN_CONFIG in user-configurable OTP, at Z1_OTP_BOOTPIN_CONFIG or Z2_OTP_BOOTPIN_CONFIG in user DCS OTP. During debugging, EMU-BOOTPIN_CONFIG is the emulation equivalent of Z1_OTP_BOOTPIN_CONFIG/Z2_OTP_BOOTPIN_CONFIG and can be programmed to test different boot modes without writing OTP. The device can be programmed to use 0, 1, 2, or 3 boot mode select pins.

Zero-pin boot: Enabling Zero-pin Boot and Flash Boot in OTP prevents all pin-based external loader options (for example, UART and CAN).

Table 23 BOOTPIN_CONFIG Bit Fields

Bit	Name	Description
7:0	Boot mode select pin 0 (BMSP0)	Set to the GPIO pin used during boot (up to 255). 0x0 = GPIO0; 0x01 = GPIO1, etc. If all other BMSPs are also set to 0xFF, 0xFF is invalid and factory-default BMSP0 is selected. If any other BMSP is not 0xFF, setting a BMSP to 0xFF disables that BMSP.
15:8	Boot mode select pin 1 (BMSP1)	See the BMSP0 description
23:16	Boot mode select pin 2 (BMSP2)	See the BMPS0 description
31:24	Key	Write 0x5A to these 8 bits to tell the boot ROM that the bits in this register are valid.

Note: The following GPIOs cannot be used as BMSPs. If selected for a BMSP, the boot ROM automatically selects the factory-default GPIO (the factory default for BMSP2 is 0xFF, which disables the BMSP).

- GPIO 36
- GPIO 38
- GPIO 47
- GPIO 50 to 223
- GPIO 225
- GPIO 229 to 241
- GPIO 243

Table 24 Individual Boot Mode Select Pin Decoding

BOOTPIN_CONFIG key	BMSP0	BMSP1	BMSP2	Implemented boot mode
!= 0x5A	Don't care	Don't care	Don't care	Boot defined by factory-default BMSPs (GPIO24, GPIO32)
= 0x5A	0xFF	0xFF	0xFF	Boot defined in the boot table for boot mode 3 (All BMSPs disabled)
	Valid GPIO	0xFF	0xFF	Boot defined by the BMSP0 value (BMSP1 and BMSP2 disabled)
	0xFF	Valid GPIO	0xFF	Boot defined by the BMSP1 value (BMSP0 and BMSP2 disabled)
	0xFF	0xFF	Valid GPIO	Boot defined by the BMSP2 value (BMSP0 and BMSP1 disabled)
	Valid GPIO	Valid GPIO	0xFF	Boot defined by BMSP0 and BMSP1 values (BMSP2 disabled)
	Valid GPIO	0xFF	Valid GPIO	Boot defined by BMSP0 and BMSP2 values (BMSP1 disabled)
	0xFF	Valid GPIO	Valid GPIO	Boot defined by BMSP1 and BMSP2 values (BMSP0 disabled)
	Valid GPIO	Valid GPIO	Valid GPIO	Boot defined by BMSP0, BMPS1, and BMSP2 values

4.8.1.2. Configuring Alternate Boot Mode Options

This section describes configuration of the BOOTDEF boot definition table and associated boot options. The 64-bit location is in user-configurable DCS OTP at Z1_OTP_BOOTDEF_LOW and Z1_OTP_BOOTDEF_HIGH. During debugging, EMU_BOOTDEF_LOW and EMU_BOOTDEF_HIGH are their emulation equivalents and can be programmed to test different boot mode options without writing OTP. The customizable boot definition table range depends on the number of boot mode select pins used.

Note: When configuring Z2-OTP-BOOTPIN-CONFIG, Z2-OTP-BOOTDEF-LOW and Z2-OTP-BOOTDEF-HIGH are used instead of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH. See Section 4.8.1.1 for BOOTPIN_CONFIG usage details.

Table 25 BOOTDEF Bit Fields

BOOTDEF name	Byte location	Name	Description
BOOT_DEF0	7:0	BOOT_DEF0 mode and options	Sets the boot mode and boot mode options. These can include changing GPIOs for a boot peripheral or specifying a different Flash entry point. Any unsupported boot mode causes a device reset. See the GPIO Assignment section for valid BOOTDEF values.
BOOT_DEF1	15:8	BOOT_DEF1 mode and options	See the BOOT_DEF0 description.
BOOT_DEF2	23:16	BOOT_DEF2 mode and options	
BOOT_DEF3	31:24	BOOT_DEF3 mode and options	
BOOT_DEF4	39:32	BOOT_DEF4 mode and options	
BOOT_DEF5	47:40	BOOT_DEF5 mode and options	
BOOT_DEF6	55:48	BOOT_DEF6 mode and options	
BOOT_DEF7	63:56	BOOT_DEF7 mode and options	

Status and flag information generated during BOOT is stored at the start of DTCM for subsequent Boot Loader or application queries. Boot flags and storage addresses are listed below:

Table 26 BOOT Flags

Content	Address	Description
BOOT Progress Indicator	0x2000_0000	BOOT execution progress
BOOT Mode Indicator	0x2000_0004	BOOT MODE selected by the bootloader from boot configuration and GPIO values.
MBIST Result(POR)	0x2000_0008	MBIST result at POR startup
Flash 1-bit ECC Error Address0	0x2000_000C	Address of Flash Bank0 single-bit ECC error
Flash 1-bit ECC Error Address1	0x2000_0010	Address of Flash Bank1 single-bit ECC error
CBROM_NMI_Status	0x2000_0014	NMI_FLG on NMI entry
Reserved	0x2000_0018	Reserved
Reserved	0x2000_001C	Reserved

4.8.1.3. GPIO Assignment

This section details the GPIOs and boot options for each boot mode configured in BOOT_DEFx at Z1_OTP_BOOTDEF_LOW and Z1_OTP_BOOTDEF_HIGH. See Configuring Alternate Boot Mode Select Pins for BOOT_DEFx configuration. When selecting a boot option, verify that the required pins are available in the pin mux options of the specific device package.

Table 27 UART Boot Options

Option	BOOTDEFx value	UARTA_TX GPIO	UARTA_RX GPIO
0 (default)	0x01	GPIO29	GPIO28
1	0x21	GPIO1	GPIO0
2	0x41	GPIO8	GPIO9
3	0x61	GPIO7	GPIO3
4	0x81	GPIO16	GPIO3

Note: Pull-up resistors are enabled on UARTA_TX and UARTA_RX.

Table 28 CAN Boot Options

Option	BOOTDEFx value	CANA_TX GPIO	CANA_RX GPIO
0 (default)	0x02	GPIO7	GPIO5
1	0x22	GPIO32	GPIO33
2	0x42	GPIO2	GPIO3
3	0x62	GPIO13	GPIO12

Note: Pull-up resistors are enabled on CANA_TX and CANA_RX.

Table 29 CAN FD Boot Options

Option	BOOTDEFx value	CANFDA_TX GPIO	CANFDA_RX GPIO
0 (default)	0x08	GPIO1	GPIO0
1	0x28	GPIO4	GPIO5
2	0x48	GPIO13	GPIO12

Note: Pull-up resistors are enabled on CANFDA_TX and CANFDA_RX.

Table 30 Wait Boot Options

Option	BOOTDEFx value	Watchdog status
0	0x04	Enabled
1	0x24	Disabled

Table 31 SPI Boot Options

Option	BOOTDEFx value	SPIA_SIMO	SPIA_SOMI	SPIA_CLK	SPIA_STE
1	0x06	GPIO7	GPIO1	GPIO3	GPIO5
2	0x26	GPIO16	GPIO1	GPIO3	GPIO0
3	0x46	GPIO8	GPIO10	GPIO9	GPIO11
4	0x66	GPIO16	GPIO13	GPI12	GPIO29

Note: Pull-up resistors are enabled on SPIA_SIMO, SPIA_SOMI, SPIA_CLK, and SPIA_STE.

Table 32 I2C Boot Options

Option	BOOTDEFx value	I2CA_SDA GPIO	I2CA_SCL GPIO
0	0x07	GPIO0	GPIO1
1	0x27	GPIO32	GPIO33
2	0x47	GPIO5	GPIO4

Note: Pull-up resistors are enabled on I2CA_SDA and I2CA_SCL.

4.8.2. Entry Addresses

Table 33 Flash Entry Address Map

Option	BOOTDEFx value	Flash sector	Address
0	0x03	BANK0 Secter0 (single-bank mode) BANK0 Secter0 (dual-bank mode)	0x0800_0000
1	0x23	BANK0 Sector4 (single-bank mode) BANK0 Secter8 (dual-bank mode)	0x0801_0000
2	0x43	BANK0 End of Sector7 (single-bank mode) BANK0 End of Secter15 (dual-bank mode)	0x0801_FFF0
3	0x63	BANK0 Sector8 (single-bank mode) BANK0 Secter16 (dual-bank mode)	0x0802_0000
4	0x83	BANK0 Sector12 (single-bank mode) BANK0 Secter24 (dual-bank mode)	0x0803_0000
5	0xA3	BANK0 End of Sector15 (single-bank mode) BANK0 End of Secter31 (dual-bank mode)	0x0803_FFF0

Table 34 RAM Entry Address

Option	BOOTDEFx value	RAM entry point address
0	0x05	0x0(ITCM)
1	0x25	0x2000_0800(DTCM)

4.8.3. MPOST Configuration in GPREG2

Bit-field descriptions for user-configurable OTP locations Z1-OTP-BOOTGPREG2 or Z2-OTP-BOOT-GPREG2.

Table 35 DCS ZONE GPREG2 Bit Fields

Bit field	Name	Description	Boot ROM action
31:24	KEY	0x5A indicates that the bits in this register are valid. Otherwise, the register is invalid and BOOT ignores it.	BOOT checks for 0x5A. If present, it performs the operations specified by the bit fields; otherwise, it ignores the register and skips the operations.
23:11	Reserved	Reserved	No Action

<table>
<tr><td>10:6</td><td>POR BIST Control</td><td>Specifies whether Memory BIST is performed on a block at POR.
0: Perform Memory BIST
. 1: Do not perform Memory BIST
. Bit[10]: ROM BIST control.
Bit[9]: CACHE BIST control.
Bit[8]: CANA BIST control.
Bit[7]: CANFDA BIST control.
Bit[6]: TCM BIST control</td><td>BOOT enables the corresponding Memory BIST according to each bit, polls the hardware BIST status, and reads and records the results after completion.</td></tr>
<tr><td rowspan="4">5:4</td><td rowspan="4">ERROR_STS_PINConfig</td><td>0x0: GPIO24, MUX Option 13</td><td rowspan="4">Specifies the GPIO for ERROR_STS output. BOOT configures the corresponding GPIO MUX accordingly.</td></tr>
<tr><td>0x1: GPIO28, MUX Option 13</td></tr>
<tr><td>0x2: GPIO29, MUX Option 13</td></tr>
<tr><td>0x3: ERROR_STS disabled</td></tr>
<tr><td>3:0</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
</table>

Z1-GPREG2 shares ECC with Z1-GPREG1, so users can program both locations in user OTP together.

4.8.4. M-POST Results

M-POST execution status is available in bit 10 of BROM_STATUS at 0x2000_0000. The M-POST test function return value is stored at 0x2000_0008 and provides execution details. Decode these values using the following table.

Bit field	Status	Description
31:29	Reserved	Reserved
28	ROM BIST Result flag	1: ROM BIST executed and completed on time (bit[20] indicates pass/fail) 0: ROM BIST executed; timeout
27	CACHE BIST Result flag	1: CACHE BIST executed, passed, or not executed (bit[19] indicates pass/fail) 0: CACHE BIST executed; timeout
26	CANA RAM BIST Result flag	1: CANA RAM BIST executed and completed on time (bit[18] indicates pass/fail) 0: CANA RAM BIST executed; timeout
25	CANFDA RAM BIST Result flag	1: CANFDA RAM BIST executed and completed on time (bit[17] indicates pass/fail) 0: CANFDA RAM BIST executed; timeout
24	TCM BIST Result flag	1: TCM BIST executed and completed on time (bit[16] indicates pass/fail) 0: TCM BIST executed; timeout
23:21	Reserved	
20	ROM BIST Result flag	1: ROM BIST passed or not executed

Bit field	Status	Description
		0: ROM BIST executed; timeout
19	CACHE BIST Result flag	1: CACHE BIST passed or not executed 0: CACHE BIST failed
18	CANA RAM BIST Result flag	1: CANA RAM BIST passed or not executed 0: CANA RAM BIST executed; timeout
17	CANFDA RAM BIST Result flag	1: CANFDA RAM BIST passed or not executed 0: CANFDA RAM BIST executed; timeout
16	TCM BIST Result flag	1: TCM BIST passed or not executed 0: TCM BIST executed; timeout
15:5	Reserved	
4	ROM BIST Execute Indicator	1: ROM BIST executed 0: ROM BIST not executed
3	CACHE BIST Execute Indicator	1: CACHE BIST executed 0: CACHE BIST not executed
2	CANA RAM BIST Execute	1: CANA RAM BIST executed 0: CANA RAM BIST not executed
1	CANFDA RAM BIST Execute	1: CANFDA RAM BIST executed 0: CANFDA RAM BIST not executed
0	TCM BIST Execute	1: TCM BIST executed 0: TCM BIST not executed

4.9. Dual-Code Security Module (DCS)

The dual-code security module (DCS) prevents unauthorized access to and inspection of on-chip secure memory and other secure resources. Secure means access to these memories and resources is blocked; non-secure means access is allowed. Refer to the G32R502 DCS User Manual for more information.

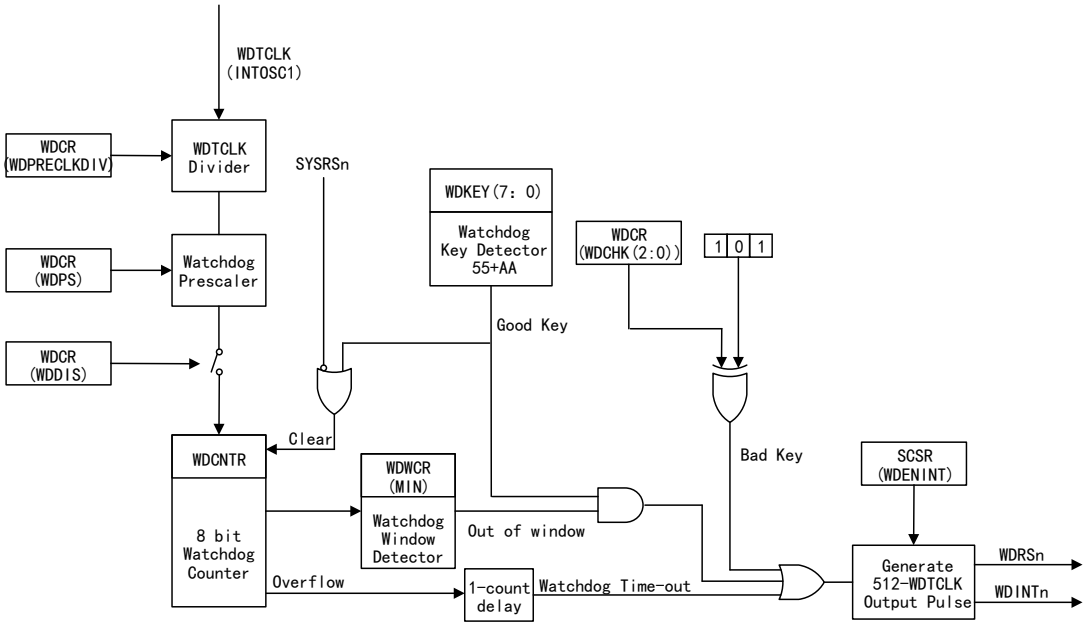
The dual-code security module (DCS) enforces security. The first line of defense protects the chip boundary and should always be enabled. Additional security features support code partitioning, as follows:

- Chip boundary protection
  - JTAGLOCK: Enabling JTAGLOCK in USER OTP disables JTAG access to device resources (for example, through a debug probe).
- Code security: Protects code zones. Each zone has dedicated secure resources (OTP memory and secure ROM) and assigned secure resources (RAM and Flash sectors).

4.10. Watchdog

The watchdog module provides an optional lower reset-limit register, disabled by default. The watchdog is clocked from an internal oscillator through an optional divider.

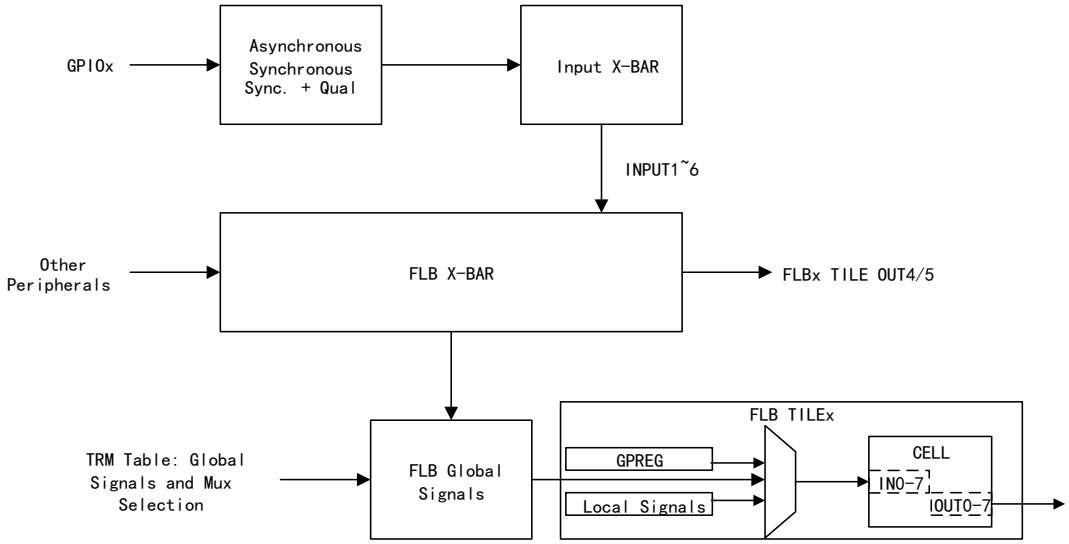
Figure 10 Block Diagram



4.11. Flexible logic block (FLB)

The flexible logic block (FLB) is a set of configurable custom logic modules. It can also enhance existing peripheral interconnects, providing extensive connectivity for on-chip control peripherals such as PWM and QEP.

Figure 11 GPIO-to-FLB TILE Connections



5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Measured under recommended operating conditions, unless otherwise specified (1) (2)

Table 36 Absolute Maximum Ratings

		Min	Max	Unit
Supply voltage	VDD relative to VSS	-0.3	1.5	V
	VDDIO relative to VSS	-0.3	4.6	
	VDDA relative to VSSA	-0.3	4.6	
Input voltage	VIN (3.3V)	-0.3	4.6	V
Output voltage	VO	-0.3	4.6	V
Input clamp current	Digital/analog input (per pin), IIK (VIN < VSS/VSSA or VIN > VDDIO/VDDA) (4)	-20	20	mA
	Total for all inputs, IIKTOTAL (VIN < VSS/VSSA or VIN > VDDIO/VDDA)	-20	20	
Output current	Digital output (per pin), IOUT	-20	20	mA
Operating junction temperature	TJ	-40	155	℃
Storage temperature (3)	Tstg	–65	150	℃

Note:

(1) Operation beyond the absolute maximum ratings may damage the device. These ratings do not imply functional operation at these or any conditions outside the recommended operating conditions. Operation outside the recommended conditions, even within the absolute maximum ratings, may not be fully functional and may affect reliability, functionality, performance, and device lifetime.

(2) All voltage values are referenced to VSS unless otherwise specified.

(3) Extended storage at high temperature or prolonged use at the maximum temperature may reduce overall device lifetime. See the Semiconductor and IC Package Thermal Metrics application report for more information.

(4) The continuous clamp current is ±2mA per pin. Do not operate continuously under this condition, as VDDIO/VDDA may rise internally and affect other electrical specifications.

5.2. EMC

5.2.1. Electrostatic Discharge Immunity (ESD)

Table 37 ESD Absolute Maximum Ratings

Symbol	Parameter	Conditions	Class	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 ℃, Standard: ANSI/ESDA/JEDEC JS-001	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charged device model)	T_A = +25 ℃, Standard: ANSI/ESDA/JEDEC JS-002	C3	1000	

Note: Based on comprehensive evaluation; not tested in production.

5.2.2. Latch up

Latch-up occurs in CMOS integrated circuits when interacting parasitic bipolar junction transistors (BJTs) form a low-impedance path between VDD and GND, resulting in a large current that may damage the chip. It mainly occurs in I/O circuits susceptible to external interference, but may also occur in internal circuits.

Table 38 Latch-up

Symbol	Parameter	Conditions	Type
LU	Latch-up	T_A = 105℃, standard: JEDEC JESD78	Class II A (±200mA)

Note: Based on comprehensive evaluation; not tested in production.

5.3. Recommended Operating Conditions

Table 39 Recommended Operating Conditions

		Min	Typ	Max	Unit
Device supply voltage, VDDIO and VDDA	Internal BOR enabled (3)	VBOR-VDDIO(MAX) + VBOR-GB (2)	3.3	3.63	V
	Internal BOR disabled	3.1	3.3	3.63	
Device supply voltage, VDD		1	1.1	1.2	V
Device ground, VSS			0		V
Analog ground, VSSA			0		V
SR_{SUPPLY}	Supply voltage ramp rate for VDDIO, VDD, and VDDA relative to VSS (4)				
V_{IN}	Digital input voltage	VSS – 0.3		VDDIO + 0.3	V
Analog input voltage		VSSA – 0.3		VDDA + 0.3	V

		Min	Typ	Max	Unit
Junction temperature, T_J (1)	-	-40		150	℃
Free-air temperature, T_A	xxx7 devices	-40		105	℃
	xxx8 devices	-40		125	℃

Note:

(1) Extended operation above T_J = 105°C reduces device lifetime. See Calculating the Useful Lifetime of Embedded Processors for more information.

(2) See the Power Management Module (PMM) section.

(3) Internal BOR is enabled by default.

(4) See the Power Management Module Operating Conditions table.

5.4. Power Consumption Summary

Current values in this subsection apply only to the specified test conditions and are not absolute maximum values. Actual device current varies with application code and pin configuration.

5.4.1. System Current Consumption - VREG Enabled

Measured under recommended operating conditions, unless otherwise specified. Temperatures shown are T_J.

Table 40 System Current Consumption - VREG Enabled

Parameter		Test conditions		Typ	Unit
Operating mode					
IDDIO	VDDIO current consumption during operation	Estimated current for a typical heavily loaded application. Actual current varies with system activity, I/O electrical loading, and switching frequency. Includes core supply current with the internal Vreg enabled. - Flash powered on - X1/X2 crystal oscillator powered on - PLL enabled, SYSCLK = maximum device frequency - Analog modules powered on - Outputs static with no DC load - Inputs static high or low - I/O pins drive no external components - Clocks enabled for all peripherals	-40℃	63	mA
			25℃	64.2	mA
			105℃	72.5	mA
			145℃	87.3	mA
IDDA	VDDA current consumption during operation		-40℃	11.1	mA
			25℃	11.2	mA
			105℃	11.4	mA
			145℃	11.8	mA
Idle mode					

IDDIO	VDDIO current consumption in idle mode	- CPU idle - X1/X2 crystal oscillator powered on - PLL enabled, SYSCLK = maximum device frequency - Analog modules powered down - Outputs static with no DC load - Inputs static high - I/O pins drive no external components	-40℃	28.9	mA
			25℃	29.7	mA
			105℃	37.1	mA
			145℃	51.2	mA
IDDA	VDDA current consumption in idle mode		-40℃	7.3	mA
			25℃	7.4	mA
			105℃	7.5	mA
			145℃	7.7	mA
Halt mode					
IDDIO	VDDIO current consumption in halt mode	- CPU in halt mode - X1/X2 powered down - PLL disabled - Analog modules powered down - Outputs static with no DC load - Inputs static high - I/O pins drive no external components	-40℃	0.4	mA
			25℃	0.8	mA
			105℃	6.8	mA
			145℃	19.6	mA
IDDA	VDDA current consumption in halt mode		-40℃	0.1	mA
			25℃	0.1	mA
			105℃	0.1	mA
			145℃	0.1	mA

5.4.2. System Current Consumption - VREG Disabled

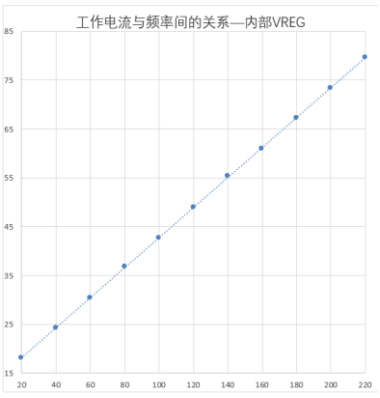
Measured under recommended operating conditions, unless otherwise specified. Temperatures shown are T_J.

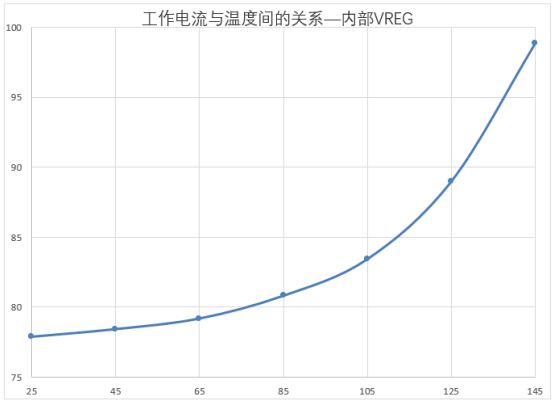
Table 41 System Current Consumption - VREG Disabled

Parameter		Test conditions		Typ	Unit
Operating mode					
IDD	VDD current consumption during operation	Estimated current for a typical heavily loaded application. Actual current varies with system activity, I/O electrical loading, and switching frequency. Includes core supply current with the internal Vreg enabled. - Flash powered on - X1/X2 crystal oscillator powered on - PLL enabled, SYSCLK = maximum device frequency - Analog modules powered on - Outputs static with no DC load - Inputs static high or low	-40℃	62.5	mA
			25℃	63.3	mA
			105℃	69.4	mA
			145℃	81.1	mA
IDDIO	VDDIO current consumption during operation		-40℃	1.2	mA
			25℃	1.3	mA
			105℃	1.4	mA
			145℃	1.5	mA
IDDA	VDDA current consumption during operation		-40℃	10.7	mA
			25℃	10.8	mA
			105℃	11.0	mA
			145℃	11.3	mA

		- I/O pins drive no external components - Clocks enabled for all peripherals			
Idle mode					
IDD	VDD current consumption in idle mode	- CPU idle - X1/X2 crystal oscillator powered on - PLL enabled, SYSCLK = maximum device frequency - Analog modules powered down - Outputs static with no DC load - Inputs static high - I/O pins drive no external components	-40℃	28.5	mA
			25℃	29.1	mA
			105℃	35.6	mA
			145℃	47.9	mA
IDDIO	VDDIO current consumption in idle mode		-40℃	1.2	mA
			25℃	1.3	mA
			105℃	1.4	mA
			145℃	1.4	mA
IDDA	VDDA current consumption in idle mode		-40℃	7.0	mA
			25℃	7.1	mA
			105℃	7.2	mA
			145℃	7.4	mA
Halt mode					
IDD	VDD current consumption in halt mode	- CPU in halt mode - X1/X2 powered down - PLL disabled - Analog modules powered down - Outputs static with no DC load - Inputs static high - I/O pins drive no external components	-40℃	0.4	mA
			25℃	0.9	mA
			105℃	7.4	mA
			145℃	20.1	mA
IDDIO	VDDIO current consumption in halt mode		-40℃	0.4	mA
			25℃	0.4	mA
			105℃	0.4	mA
			145℃	0.4	mA
IDDA	VDDA current consumption in halt mode		-40℃	0.1	mA
			25℃	0.1	mA
			105℃	0.1	mA
			145℃	0.1	mA

5.4.3. Current Consumption Diagram





Above is a typical representation of the relationship between operating frequency / temperature

and current consumption with VREG enabled.

5.4.4. Reducing Current Consumption

The device provides the following ways to reduce current consumption:

- To further reduce current during application idle periods, enter either of the two low-power modes: idle or halt.
- Power down the Flash module when code runs from RAM.
- Disable pull-up resistors on pins configured as outputs.
- Each peripheral has a separate clock enable bit (PCLKCRx). Disabling clocks to unused peripherals reduces current consumption. The following table lists typical current reductions achieved by disabling clocks through the PCLKCRx registers.
- To reduce VDDA current consumption in LPM, ensure that each module is powered down as described in the Analog-to-Digital Converter (ADC) chapter of the *G32R502 User Manual.*

5.4.4.1. Typical Current Reduction per Disabled Peripheral

For peripherals with multiple instances, the listed current applies to all modules.

Table 42 Typical Current Reduction per Disabled Peripheral

Peripheral	IDDIO current reduction (mA)
ADC	2.32
COMP	3.27
CPU counter	0.4
CAN	1.15
CAN FD	0.81
DCCOMP	0.03
CAP	0.41
QEP	0.21
PWM	9.66
HRPWM	0.24
LIN	0.21
UART	0.28
SPI	0.13
PMBUS	0.33
I2C	0.28
FLB	5.33

Note: This is the current drawn by the digital portion of each module.

5.5. Electrical Characteristics

Measured under recommended operating conditions, unless otherwise specified

Table 43 Digital and Analog I/O

Parameter			Test conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MIN	VDDIO * 0.8			V
			I_{OH}=-100μ A	VDDIO – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = IOL maximum			0.4	V
			I_{OL} = 100μA			0.2	
I_{OH}	High-level source current for all output pins		DS0/DS1=00@2mA DS0/DS1=01@4mA DS0/DS1=10@8mA DS0/DS1=11@12mA	-2 -4 -8 -12			mA
I_{OL}	Low-level sink current for all output pins		DS0/DS1=00@2mA DS0/DS1=01@4mA DS0/DS1=10@8mA DS0/DS1=11@12mA			2 4 8 12	mA
R_{OH}	High-level output impedance for all output pins		V_{OH}=VDDS-0.4V	50	65	96	Ω
R_{OL}	Low-level output impedance for all output pins		V_{OL}=0.4V	48	60	84	Ω
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
$V_{HYSTERESIS}$	Input hysteresis (AIO)			125			mV
	Input hysteresis (GPIO)			125			
$I_{PULLDOWN}$	Input current	Pins with pull-down	VDDIO = 3.3V V_{IN} = VDDIO		120		μA
I_{PULLUP}	Input current	Digital inputs with pull-up enabled (1)	VDDIO = 3.3V V_{IN} = 0V		160		μA
$R_{PULLDOWN}$	Weak pull-down resistance			22.66	31.49	61.55	kΩ
R_{PULLUP}	Weak pull-up resistance			19.89	29.45	53.63	kΩ
I_{LEAK}	Pin leakage current	Digital inputs	Pull-up and output disabled, 0V ≤ V_{IN} ≤ VDDIO			0.1	μA
		Analog pins	Analog driver disabled, 0V ≤ V_{IN} ≤ VDDA			0.1	μA
C_I	Input capacitance	Digital inputs			2		pF
		Analog pins					

Parameter			Test conditions	Min	Typ	Max	Unit
		(2)					
VREG and BOR							
V_{REG}/ POR/BOR(3)							

Note:

(1) See the Pins with Internal Pull-up and Pull-down Resistors table for a list of pins with pull-up or pull-down resistors.

(2) Analog pins are specified separately; see the Parasitic Capacitance per Channel table in the ADC Input Model section.

(3) See the Power Management Module (PMM) section.

5.6. Thermal Resistance Characteristics

Table 44 LQFP80 Package Thermal Characteristics

		°C/W(1)
RΘ JC	Junction-to-case thermal resistance, top	13.07
	Junction-to-case thermal resistance, bottom	Not applicable
RΘ JB	Junction-to-board thermal resistance	26.91
RΘ JA (high-k PCB)	Junction-to-ambient thermal resistance	41.13

Note:

(1) These values are based on a JEDEC-defined 2S2P system, except Theta JC [RΘJC], which is based on a JEDEC-defined 1S0P system, and vary with environment and application. For more information, see the following EIA/JEDEC standards:

- JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements

Table 45 LQFP64 Package Thermal Characteristics

		°C/W(1)
RΘ JC	Junction-to-case thermal resistance, top	15.06
	Junction-to-case thermal resistance, bottom	Not applicable
RΘ JB	Junction-to-board thermal resistance	22.45
RΘ JA (high-k PCB)	Junction-to-ambient thermal resistance	45.98

Note:

(1) These values are based on a JEDEC-defined 2S2P system, except Theta JC [RΘJC], which is based on a JEDEC-defined 1S0P system, and vary with environment and application. For more information, see the following EIA/JEDEC standards:

- JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements

Table 46 HTQFP48 Package Thermal Characteristics

		°C/W(1)
RΘ JC	Junction-to-case thermal resistance, top	13.61
	Junction-to-case thermal resistance, bottom	Not applicable
RΘ JB	Junction-to-board thermal resistance	6.9
RΘ JA (high-k PCB)	Junction-to-ambient thermal resistance	29.01

Note:

(1) These values are based on a JEDEC-defined 2S2P system, except Theta JC [RΘJC], which is based on a JEDEC-defined 1S0P system, and vary with environment and application. For more information, see the following EIA/JEDEC standards:

- JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements

Table 47 VQFN32 Package Thermal Characteristics

		°C/W(1)
RΘ JC	Junction-to-case thermal resistance, top	21.24
	Junction-to-case thermal resistance, bottom	1.72
RΘ JB	Junction-to-board thermal resistance	10.02
RΘ JA (high-k PCB)	Junction-to-ambient thermal resistance	39.87

Note:

(1) These values are based on a JEDEC-defined 2S2P system, except Theta JC [RΘJC], which is based on a JEDEC-defined 1S0P system, and vary with environment and application. For more information, see the following EIA/JEDEC standards:

- JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements

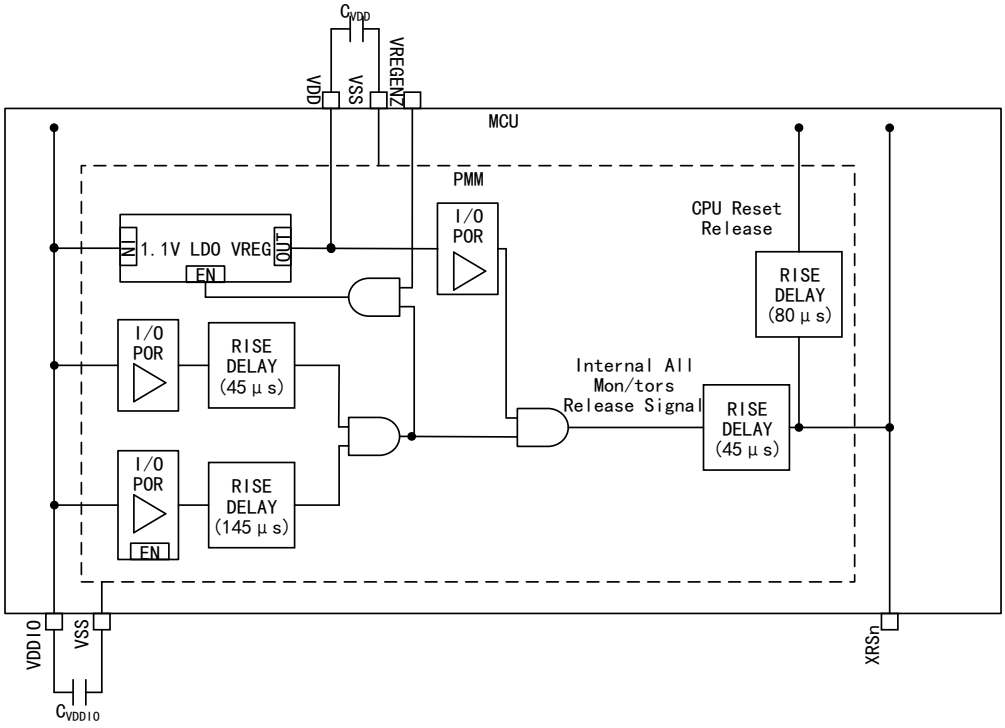
5.7. System

5.7.1. Power Management Module (PMM)

The Power Management Module (PMM) handles all power management functions required for device operation.

The following figure shows the PMM block diagram. PMM contains several subcomponents, described in the following sections.

Figure 12 PMM Block Diagram



5.7.1.1. Supply Rail Monitors

PMM provides voltage monitors on the supply rails. During power-up, XRSn is released high when voltages exceed the specified thresholds. These monitors can also drive XRSn low if any voltage falls below its threshold. The following sections describe the voltage monitors.

Note: If a voltage monitor does not support application monitoring, use an external supervisor when supply monitoring is required during operation. All three monitors, I/O POR, I/O BOR, and VDD POR, must release their outputs before device

operation starts (XRSn goes high). If any monitor trips, XRSn is driven low. I/Os remain in a high-impedance state whenever any voltage monitor trips.

I/O POR Monitor

Power-on reset (I/O POR) monitors the VDDIO rail and is the first VDDIO monitor to release during power-up.

I/O BOR Monitor

Brown-out reset (I/O BOR) also monitors VDDIO and is the second VDDIO monitor to release during power-up. I/O BOR has tighter tolerance than I/O POR.

Note: I/O BOR trips and resets the device if voltage falls below the recommended operating voltage. Set VMONCTL[BORLVMONDIS] to 1 to disable this function, but only after the device has fully booted. When I/O BOR is disabled, I/O POR resets the device on a voltage drop. Its trip level is far below the minimum recommended VDDIO voltage, so I/O POR must not be used for application supply monitoring.

VDD POR Monitor

VDD POR monitors the VDD rail. During power-up, it releases when the voltage exceeds the specified VDD trip level.

Note: VDD POR is set below the minimum recommended VDD voltage. If the application requires VDD monitoring, use an external supervisor rather than relying on VDD POR.

5.7.1.2. Use of External Supervisors

VDDIO monitoring: I/O BOR supports application monitoring, so no external supervisor is required for the I/O supply rail.

VDD monitoring: VDD POR does not support application monitoring. Use an external supervisor if the application requires VDD rail monitoring.

Note: An external supervisor cannot be used with the internal VREG. If VDD monitoring is required, supply VDD externally using a package with a VREGENZ pin.

5.7.1.3. Delay Block

The delay block in the voltage monitor path delays release between the monitors and XRSn. In external VREG mode, the delay ensures voltage stability before XRSn is released. It is active only during VDDIO and VDD power-up and helps meet the minimum rail slew rates specified in Power Management Module Electrical Data and Timing.

5.7.1.4. Internal 1.1V LDO Regulator (VREG)

The internal VREG is powered by VDDIO. Connecting VREGENZ low generates the 1.1V required by the VDD pins. This eliminates an external VDD supply, but decoupling capacitors are still required on VDD for VREG stability and transient suppression. See VDD Decoupling for details.

5.7.1.5. VREGENZ

The VREG disable pin controls the internal regulator. Connect VREGENZ low to enable internal VREG. For applications using external VREG, connect VREGENZ high to disable internal VREG.

5.7.1.6. External Components

5.7.1.6.1. Decoupling Capacitors

VDDIO and VDD require decoupling capacitors for proper operation. The following sections describe the requirements.

VDDIO Decoupling

Provide at least the minimum VDDIO decoupling capacitance specified by C_{VDDIO} in Power Management Module Electrical Data and Timing. Actual capacitance depends on the VDDIO supply. Either configuration is acceptable:

- Configuration 1: Place a decoupling capacitor on each VDDIO pin according to C_{VDDIO}.
- Configuration 2: Use one decoupling capacitor equivalent to C_{VDDIO} × the number of VDDIO pins.

Note: Place the decoupling capacitor(s) close to the device pins.

VDD Decoupling

Provide at least the minimum VDD decoupling capacitance specified by C_{VDD} TOTAL in Power Management Module Electrical Data and Timing.

Either configuration is acceptable:

- Configuration 1: Divide CVDD TOTAL among the VDD pins.
- Configuration 2: Use a single decoupling capacitor of CVDD TOTAL.

Note: Place the decoupling capacitor(s) close to the device pins.

5.7.1.7. Power Sequencing

5.7.1.7.1. Supply Pin Connections

Connect all supply pins belonging to the same rail together. For example, connect all VDDIO pins together, all VDD pins together, and so on. Do not leave any supply pin floating.

Connect all 3.3V supply rails together and power them from one supply, including VDDIO and VDDA.

In internal VREG mode, connecting the VDD pins together is optional if each VDD pin has its own capacitor. See VDD Decoupling.

The on-chip analog modules have a high power supply rejection ratio (PSRR). In most cases, VDDA noise must exceed the recommended rail operating conditions before analog performance degrades. A separate VDDA supply therefore offers limited benefit. A π filter between VDDIO and VDDA can improve noise performance.

5.7.1.7.2. Signal Pin Power Sequencing

Before power-up, digital pin voltages must remain between VSS - 0.3V and VDDIO + 0.3V. Analog pin voltages, including VREFHI, must remain between VSSA - 0.3V and VDDA + 0.3V.

Drive signal pins only after XRSn goes high, assuming all 3.3V rails are connected together. This sequencing is still required if VDDIO and VDDA are not tied together.

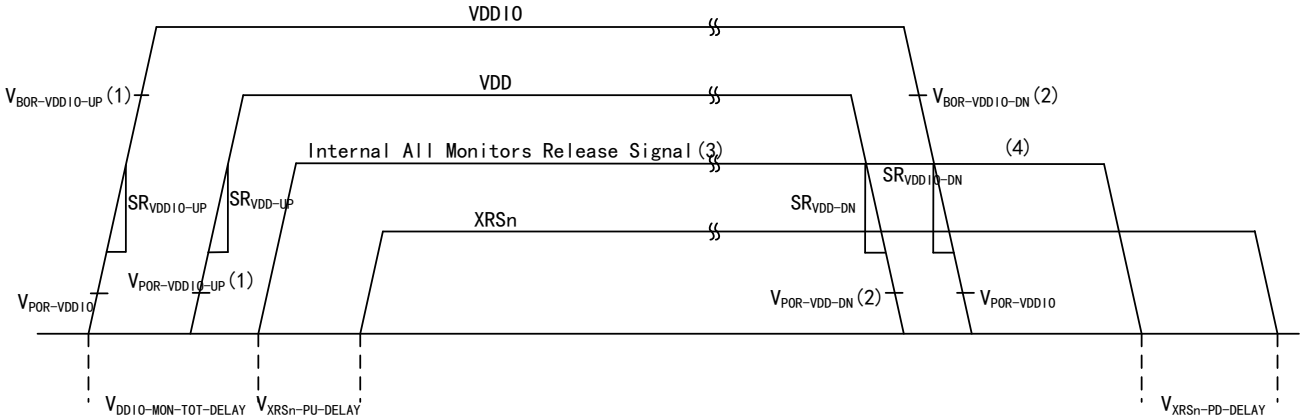
Note: Violating this sequence can cause current to flow through unintended parasitic paths, resulting in device malfunction or damage.

5.7.1.7.3. Supply Pin Power Sequencing

External VREG/VDD Mode Sequence

The following figure shows power sequencing requirements for external VREG mode. Parameter values are given in Power Management Module Electrical Data and Timing.

Figure 13 External VREG Power-up Sequence



Note:

(1) This is the trip point before XRSn is released.

(2) This is the trip point after XRSn is released.

(3) During power-up, the all-monitors-released signal goes high after all POR and BOR monitors release.

(4) During power-down, the all-monitors-released signal goes low if any POR or BOR monitor trips.

During power-up:

- First, the 3.3V VDDIO rail rises at the specified minimum slew rate.
- Next, the 1.1V VDD rail rises at the specified minimum slew rate.
- The time difference between the rise of VDDIO and VDD is specified.
- After VDDIO-MON-TOT-DELAY and VXRSN-PD-DELAY, XRSn is released and the device begins its boot sequence. An additional delay occurs between XRSn release (going high) and the boot sequence.
- The I/O BOR monitor has different release points during power-up and power-down.

- Both VDDIO and VDD must be powered before XRSn is released during power-up.

During power-down:

- There is no required order for VDDIO and VDD power-down, but minimum slew rates apply.
- The I/O BOR monitor has different release points during power-up and power-down.
- Any POR or BOR monitor trip during power-down drives XRSn low after $V_{XRSN-PD-DELAY}$.

Note:

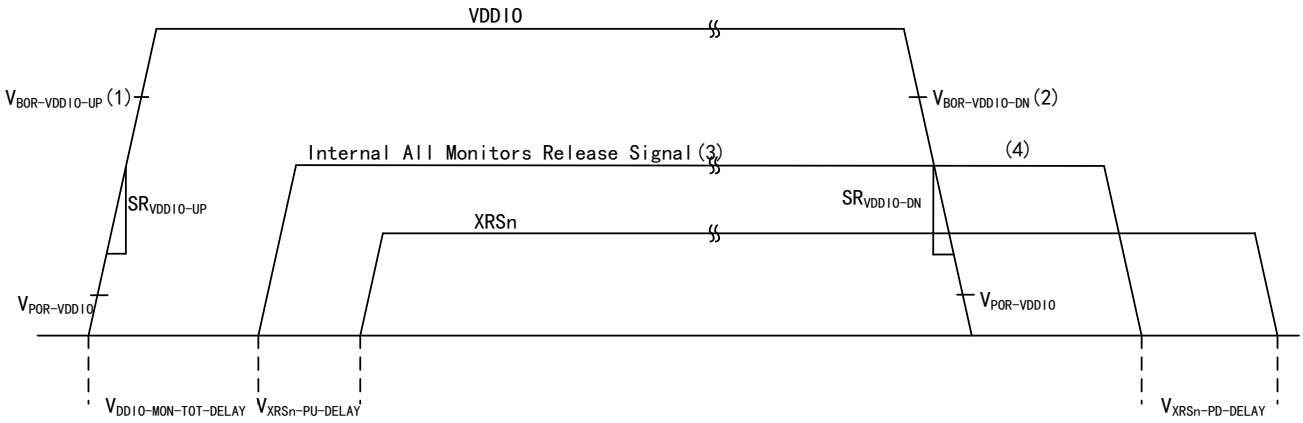
(1) The all-monitors-released signal is internal.

(2) If external circuitry, such as a supervisor, drives XRSn, the boot sequence cannot start until all internal and external sources release XRSn.

Internal VREG/VDD Mode Sequence

The following figure shows power sequencing requirements for internal VREG mode. Parameter values are given in Power Management Module Electrical Data and Timing.

Figure 14 Internal VREG Power-up Sequence



Note:

(1) This is the trip point before XRSn is released.

(2) This is the trip point after XRSn is released.

(3) During power-up, the all-monitors-released signal goes high after all POR and BOR monitors release.

(4) During power-down, the all-monitors-released signal goes low if any POR or BOR monitor trips.

During power-up:

- The 3.3V VDDIO rail rises at the specified minimum slew rate.
- The 1.1V VDD rail rises at the specified minimum slew rate.
- The time difference between the rise of VDDIO and VDD is also specified.

- After $V_{DDIO-MON-TOT-DELAY}$ and $V_{XRSN-PD-DELAY}$, XRSn is released and the device begins its boot sequence. An additional delay occurs between XRSn release (going high) and the boot sequence.
- The I/O BOR monitor has different release points during power-up and power-down.
- Both VDDIO and VDD must be powered before XRSn is released during power-up.

During power-down:

- There is no required order for VDDIO and VDD power-down, but minimum slew rates apply.
- The I/O BOR monitor has different release points during power-up and power-down.
- An I/O BOR trip drives XRSn low after $V_{XRSN-PD-DELAY}$ and powers down the internal VREG.

Note:

(1) The all-monitors-released signal is internal.

(2) If external circuitry, such as a supervisor, drives XRSn, the boot sequence cannot start until all internal and external sources release XRSn.

Power Sequencing Summary and Effects of Violations

Acceptable rail power-up sequences are summarized below. Powered up means the rail has reached its minimum recommended operating voltage. Unacceptable sequences cause reliability issues and may cause damage. For simplicity, connect all 3.3V rails together and follow Supply Pin Power Sequencing.

Table 48 External VREG Sequencing Summary

Case	Rail power-up order			Acceptable
	VDDIO	VDDA	VDD	
A	1	2	3	Yes
B	1	3	2	Yes
C	2	1	3	-
D	2	3	1	-
E	3	2	1	-
F	3	1	2	-
G	1	1	2	Yes
H	2	2	1	-

Table 49 Internal VREG Sequencing Summary

Case	Rail power-up order		Acceptable
	VDDIO	VDDA	
A	1	2	Yes
B	2	1	-
C	1	1	Yes

Note: Power the on-chip analog modules only after VDDA reaches its minimum recommended operating voltage.

Supply Slew Rate

- VDDIO has a minimum slew rate requirement.

If this requirement is not met, XRSn may toggle several times before VDDIO passes the I/O BOR region. This generally does not affect the device because boot starts only after XRSn is stably high. However, if XRSn resets other ICs, meet the slew rate requirement to prevent such toggling.

- VDD has a minimum slew rate requirement in external VREG mode.

If this requirement is not met, the device may release reset and boot before VDD reaches its minimum operating voltage, causing improper operation.

If the minimum slew rate cannot be met, use a VDD supervisor to hold XRSn low until VDD exceeds the minimum operating threshold, ensuring proper device operation.

5.7.1.8. Power Management Module Electrical Data and Timing

Table 50 Power Management Module Operating Conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
General						
C_{VDDIO}	Bulk capacitance on VDDIO	Based on external power IC requirements (1)		0.1		μF
C_{VDDIO_DCAP}	Decoupling capacitor on each VDDIO pin			0.1		μF
C_{VDDA}	Capacitor on VDDA pin			2.2		μF
C_{VDD}	Bulk capacitance on VDD	LDO-only operation (2)	12	20	27	μF
C_{VDD_DCAP}	Decoupling capacitor on each VDD pin	LDO-only operation (2)	0.1		6.75	μF
$SR_{VDDIO-UP}$(4)	3.3V rail (VDDIO) ramp-up rate		82.5		363	mV/μs
$SR_{VDDIO-DN}$(4)	3.3V rail (VDDIO) ramp-down rate		80		167.3	mV/μs
External VREG						
C_{VDD} total (3) (5)	Total VDD capacitance (7)		10			μF
SR_{VDD-UP}(4)	1.1V rail (VDD) ramp-up rate		3.5		100	mV/μs
SR_{VDD-DN}(4)	1.1V rail (VDD) ramp-down rate		10		100	mV/μs
V_{DDIO} - V_{DD} delay (6)	Ramp delay between VDDIO and VDD		0		No limit	μs

Note:

(1) Bulk capacitance on this supply should meet the power IC requirements.

(2) See Internal 1.1V LDO Regulator (VREG) for details.

(3) The exact decoupling capacitance depends on the system voltage regulation solution supplying these pins.

(4) See Supply Slew Rate. A ramp rate above the maximum triggers the on-chip ESD protection.

(5) See Power Management Module (PMM) for possible total decoupling capacitance configurations.

(6) Delay between the rise of the 3.3V and 1.1V rails. See the VREG Sequencing Summary tables for allowable rail ramp sequences.

(7) Maximum capacitor tolerance is 20%.

Table 51 Power Management Module Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{VREG}	Internal regulator output	Output configured to 1.1V	1.0	1.1	1.2	V
		Output configured to 1.0V	0.9	1.0	1.1	V
$V_{VREG-PU}$	Internal regulator power-up time		210		340	μs
$V_{VREG-INRUSH}$(5)	Internal regulator inrush current		354		662	mA
$V_{POR-VDDIO}$	VDDIO power-on reset voltage	Before and after XRSn release		2.3		V
$V_{BOR-VDDIO-UP}$(1)	VDDIO brown-out reset voltage during ramp-up	Before XRSn release		2.9		V
$V_{BOR-VDDIO-DN}$(1)	VDDIO brown-out reset voltage during ramp-down	After XRSn release	2.81		3.00	V
$V_{POR-VDD-UP}$(2)	VDD power-on reset voltage during ramp-up	Before XRSn release		0.8		V
$V_{POR-VDD-DN}$(2)	VDD power-on reset voltage during ramp-down	After XRSn release		0.8		V
$V_{XRSn-PU-DELAY}$(3)	XRSn release delay after supply ramp-up	This is the final delay		248		μs
$V_{XRSn-PD-DELAY}$(4)	XRSn trip delay after supply ramp-down			26		μs
$V_{DDIO-MON-TOT-DELAY}$	Total delay in the VDDIO monitor (POR, BOR) path			318		μs
$V_{XRSn-MON-RELEASE-DELAY}$	XRSn release delay after VDD POR event	Supply within operating range		248		μs
	XRSn release delay after VDDIO BOR			586		μs
	XRSn release delay after VDDIO POR event			509		μs

Note:

(1) See the Supply Voltage figure.

(2) $V_{POR-VDD}$ does not support application monitoring and trips below the recommended operating conditions. Use an external supervisor if VDD monitoring is required.

(3) A supply is fully ramped up after crossing its rail's minimum recommended operating voltage. All POR and BOR monitors must release before this delay begins. RC network delay is added to this delay.

(4) During power-down, any POR or BOR monitor trip initiates an XRSn trip. This delay is the time between a monitor trip and XRSn going low. It varies with the supply ramp-down rate. RC network delay is added to it.

(5) This is the transient current drawn from VDDIO when internal VREG turns on. The resulting VDDIO drop may cause VREG to ramp up in steps. This does not adversely affect the device. If desired, reduce it with sufficient VDDIO decoupling capacitance or an LDO capable of supplying this transient current.

5.7.1.9. Internal Reference Supply

Table 52 Internal Reference Supply

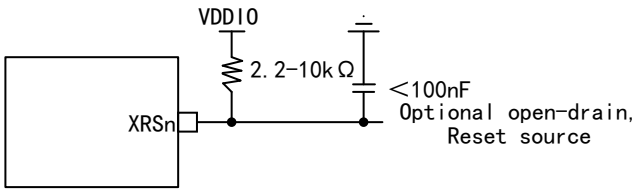
Parameter	Test conditions	Min	Typ	Max	Unit
Internal 1.65V reference voltage	-40℃~105℃	1.642	1.65	1.658	V
Internal 2.5V reference voltage	-40℃~105℃	2.488	2.5	2.512	V

5.7.2. Reset Timing

XRSn is the device reset pin. The internal POR circuit pulls XRSn low at power-up. Watchdog resets (WWDT, NMIWDT) also pull it low. External circuitry can drive the pin to reset the device.

Place a 2.2kΩ to 10kΩ resistor between XRSn and VDDIO and a capacitor smaller than 100nF between XRSn and VSS for noise filtering. These values allow the watchdog to drive XRSn correctly to VOL within 810 OSCCLK cycles during watchdog reset. The following figure shows the recommended reset circuit.

Figure 15 Reset Circuit



5.7.2.1. Reset Sources

Table 53 Reset Signals

Reset Sources	CPU core reset (CPU, FPU, VCU)	Peripheral reset	JTAG/debug logic reset	I/O	XRSn output
POR	Yes	Yes	Yes	High impedance	Yes
XRSn pin	Yes	Yes	No	High	-

Reset Sources	CPU core reset (CPU, FPU, VCU)	Peripheral reset	JTAG/debug logic reset	I/O	XRSn output
				impedance	
WDRS	Yes	Yes	No	High impedance	Yes
NMIWDRS	Yes	Yes	No	High impedance	Yes
SYSRS (debugger reset)	Yes	Yes	No	High impedance	No
SCCRESET	Yes	Yes	No	High impedance	No

Note:

(1) The $t_{h(boot-mode)}$ parameter must account for resets initiated by these sources.

(2) Some reset sources are driven internally. Some drive XRSn low to disable other devices driving the boot pins. SCCRESET and debugger reset do not drive XRSn; therefore, other system devices must not actively drive boot mode pins. Boot configuration allows boot pins to be changed in OTP.

5.7.2.2. Reset Electrical Data and Timing

Table 54 Reset (XRSn) Timing Requirements

Symbol	Parameter	Conditions	Min	Max	Unit
t_h(boot-mode)	Boot mode pin hold time		1.5		ms
$t_{w(RSL2)}$	Pulse duration, XRSn low during warm reset	All cases	74		µs
		Low-power mode used in application and SYSCLKDIV > 16	3.2*(SYSCLKDIV/16)		

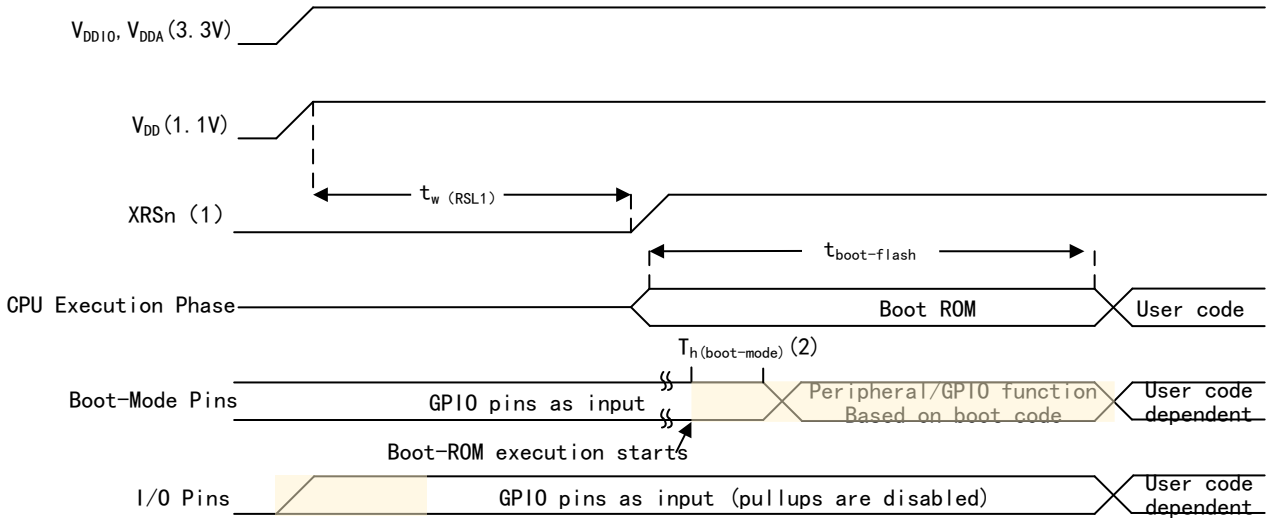
Table 55 Reset (XRSn) Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(RSL1)}$	Pulse duration	XRSn driven low by device after supply stabilization		200		µs
$t_{w(WDRS)}$	Pulse duration	Watchdog-generated reset pulse		$810t_{c(OSCCLK)}$		Period
$t_{boot-flash}$	Boot ROM execution time before the first instruction fetch from Flash				5	ms

Table 56 Reset (XRSn) I/O Filter Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(XRSn)}$	Filter duration	When I/O filter mode is selected		500		ns

Figure 16 Power-on Reset

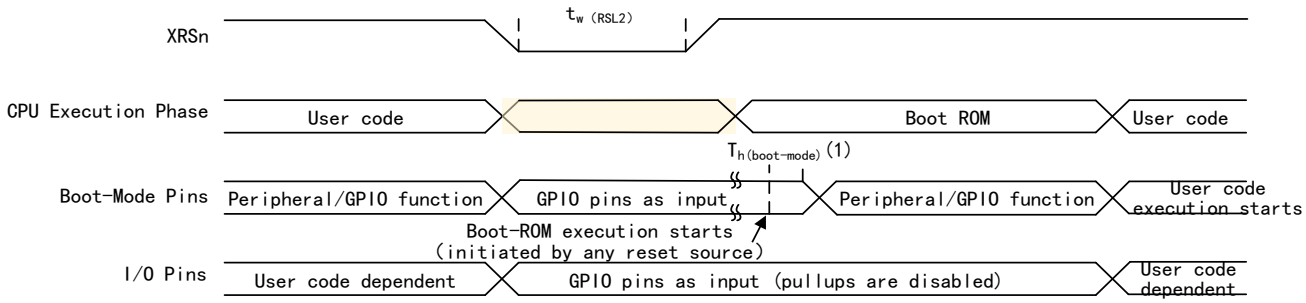


Note: SYSCLK depends on the user environment, with or without PLL enabled.

(1) XRSn may be driven externally by a supervisor or external pull-up resistor; see Pin Attributes. The on-chip POR logic holds this pin low until supplies are within the valid range.

(2) After reset from any source (see Reset Sources), boot ROM samples the boot mode pins and branches to the destination memory or boot function according to their state. If boot ROM executes after power-up in a debugger environment, execution time depends on the current SYSCLK frequency.

Figure 17 Warm Reset



Note: SYSCLK depends on the user environment, with or without PLL enabled.

(1) After reset from any source (see Reset Sources), boot ROM samples the boot mode pins and branches to the destination memory or boot function according to their state. If boot ROM executes after power-up in a debugger environment, execution time depends on the current SYSCLK frequency.

5.7.3. Clock Specifications

5.7.3.1. Clock Sources

Table 57 Available Reference Clock Sources

Clock Sources	Clocked module	Comments
INTOSC1	Can clock the following modules:	Internal oscillator 1

	Watchdog module Main PLL CPU timer 2	Zero-pin 10MHz internal oscillator
INTOSC2	Can clock the following modules: Main PLL CPU timer 2	Internal oscillator 2 Zero-pin 10MHz internal oscillator
X1(XTAL)	Can clock the following module: Main PLL CPU timer 2	External crystal or resonator connected between X1 and X2, or single-ended clock connected to X1.

Note:

(1) At reset, internal oscillator 2 (INTOSC2) is the default clock for the system PLL (OSCCLK).

Figure 18 Clock Sources

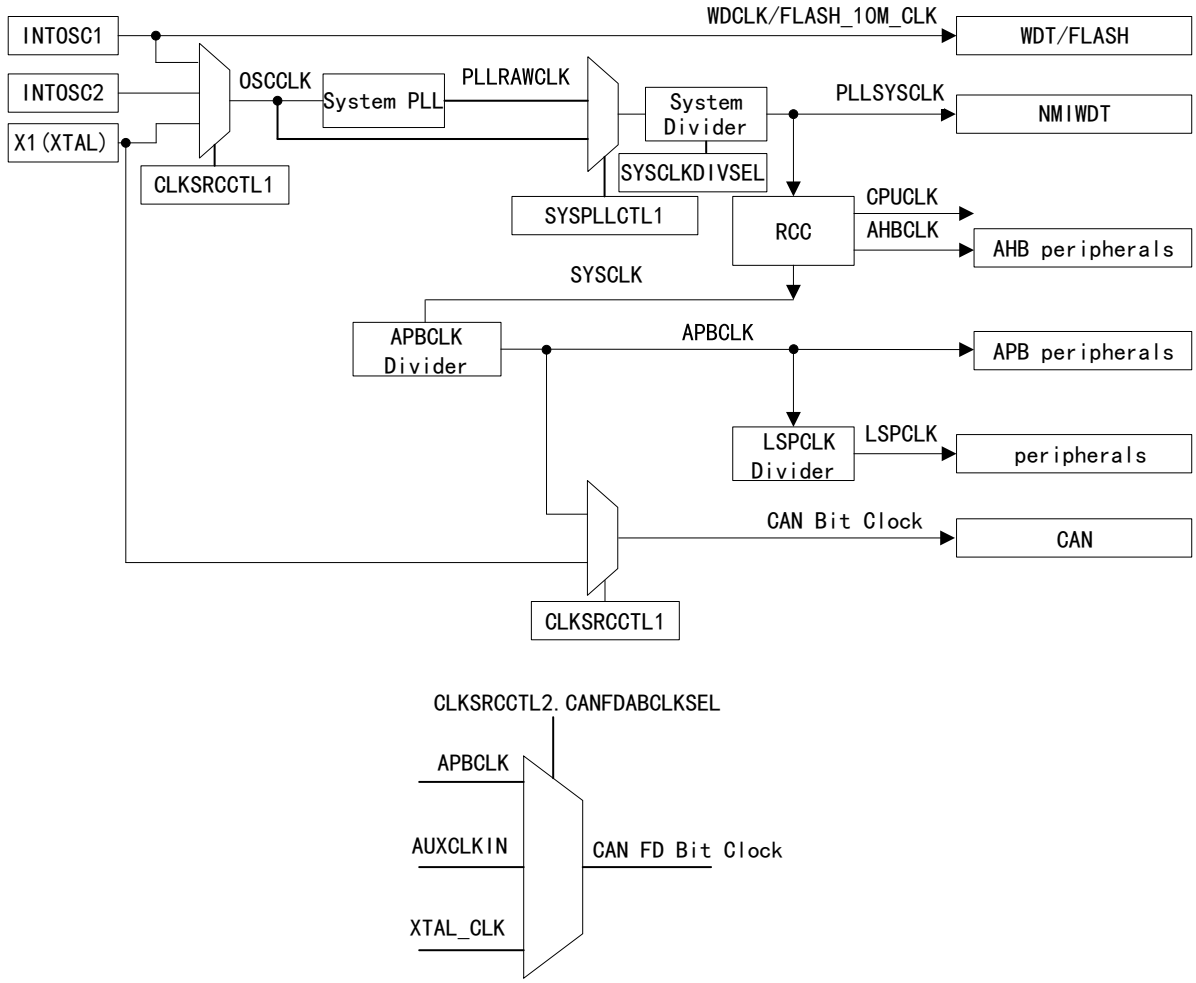
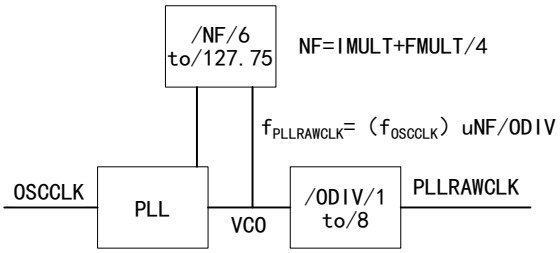


Figure 19 System PLL



5.7.3.2. Clock Frequencies, Requirements, and Characteristics

This section provides input clock frequency and timing requirements, PLL lock time, internal clock frequencies, and output clock frequencies and switching characteristics.

5.7.3.2.1. Input Clock Frequency and Timing Requirements and PLL Lock Time

Table 58 Input Clock Frequency

Symbol	Parameter	Min	Max	Unit
$f_{(XTAL)}$	Frequency, X1/X2, from external crystal or resonator	10	20	MHz
$f_{(X1)}$	Frequency, X1, from external oscillator	2	20	MHz

Table 59 XTAL Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
X1 VIL	Valid low-level input voltage	-0.3		0.3 * VDDIO	V
X1 VIH	Valid high-level input voltage	0.7 * VDDIO		VDDIO + 0.3	V

Table 60 X1 Timing Requirements

Symbol	Parameter	Min	Max	Unit
$t_{f(X1)}$	Fall time, X1		9	ns
$t_{r(X1)}$	Rise time, X1		12	ns
$t_{w(X1L)}$	Pulse duration, X1 low as percentage of $t_{c(X1)}$	45	55	%
$t_{w(X1H)}$	Pulse duration, X1 high as percentage of $t_{c(X1)}$	45	55	%

Table 61 PLL Lock Time

Symbol	Parameter	Min	Typ	Max	Unit
$t_{(PLL)}$	Lock time, main PLL		25.5μs+ 1024 * $t_{c(OSCCLK)}$		μs

5.7.3.2.2. Internal Clock Frequencies

Table 62 Internal Clock Frequencies

Symbol	Parameter	Min	Typ	Max	Unit
$f_{(SYSCLK)}$	Frequency, device (system) clock	2	160	200	MHz

Symbol	Parameter	Min	Typ	Max	Unit
$f_{(VCO)}$	Frequency, PLL VCO (before output divider) AVDD=2.9~3.6,T_j=40~125℃	100	/	400	MHz
$f_{(PLLRAWCLK)}$	Frequency, system PLL output (before SYSCLK divider)	15		200	MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		200	MHz
$f_{(APBCLK)}$	Frequency, APBCLK	2		100	MHz
$f_{(LSP)}$	Frequency, LSPCLK	2		100	MHz
$f_{(OSCCLK)}$	Frequency, OSCCLK (INTOSC1, INTOSC2, XTAL, or X1)	See the respective clock			MHz
$f_{(PWM)}$	Frequency, PWMCLK	60		200	MHz
$f_{(HRPWM)}$	Frequency, HRPWMCLK	60		200	MHz

5.7.3.2.3. Output Clock Frequencies and Switching Characteristics

Table 63 XCLKOUT Switching Characteristics

Symbol	Parameter (1)	Min	Max	Unit
$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
$t_{r(XCO)}$	Rise time, XCLKOUT		5	ns
$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H– 2(2)	H + 2(2)	ns
$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H– 2(2)	H + 2(2)	ns
$f_{(XCO)}$	Frequency, XCLKOUT		50	MHz

Note:

(1) Assume a 40pF load.

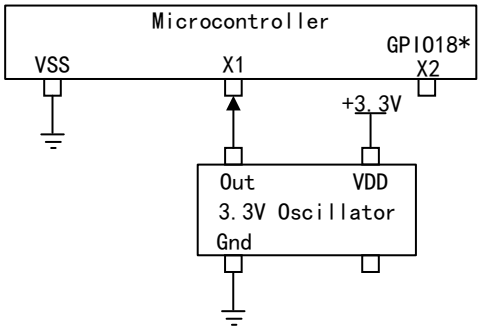
(2) H=0.5tc(XCO)

5.7.3.3. Input Clock

GPIO18* and its mux options can be used only when the system is clocked by INTOSC and X1 has an external pull-down resistor. In addition to internal zero-pin oscillators, three external clock source types are supported:

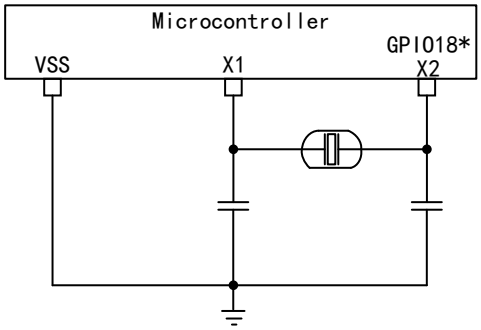
(1) Single-ended 3.3V external clock. Connect the clock to X1 and set XTALCR.SE to 1.

Figure 20 Single-ended 3.3V External Clock



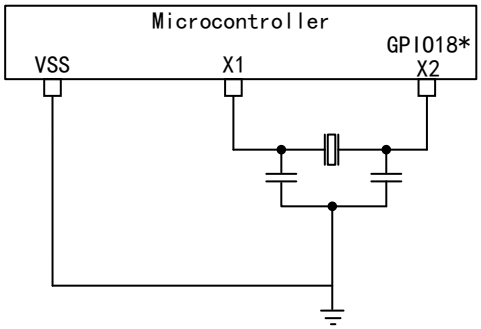
(2) External crystal. Connect the crystal between X1 and X2, with load capacitors to VSS.

Figure 21 External Crystal



(3) External resonator. Connect the resonator between X1 and X2 and its ground terminal to VSS.

Figure 22 External Resonator



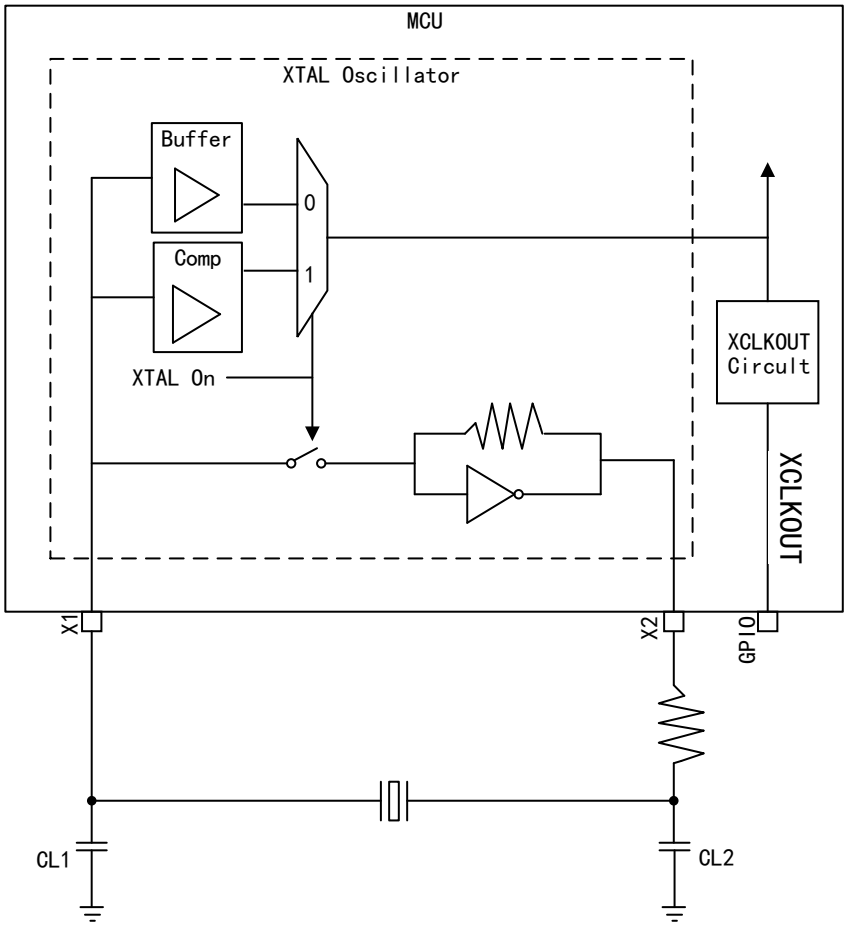
5.7.3.4. Crystal (XTAL) Oscillator

The embedded electrical oscillator generates the required system clock when paired with a compatible quartz crystal or ceramic resonator.

5.7.3.4.1. Electrical Oscillator

The electrical oscillator and a compatible crystal form a circuit that oscillates at the crystal's fundamental frequency. Due to shunt capacitance (C0) and required load capacitance (CL), it is designed for parallel resonance. The following figure shows the electrical oscillator and oscillation circuit components.

Figure 23 Electrical Oscillator Block Diagram



Operating Modes

The electrical oscillator has two operating modes: crystal mode and single-ended mode.

(1) Crystal Mode

Connect a quartz crystal with load capacitors to X1 and X2 in crystal mode.

This mode is enabled when [XTAL On] = 1 by setting XTALCR.OSCOFF = 0 and XTALCR.SE = 0. The feedback loop has an internal bias resistor. An external bias resistor would be in parallel with it, shifting the operating bias point and potentially causing waveform clipping, out-of-spec duty cycle, and reduced effective negative resistance. Do not use an external bias resistor.

In this mode, the X1 clock passes through a comparator to the rest of the device. It must meet the comparator VIH and VIL requirements in the XTAL Oscillator Characteristics table.

(2) Single-ended Mode

In single-ended mode, connect a clock to X1 and leave X2 floating. Do not use a quartz crystal in this mode.

This mode is enabled when [XTAL On] = 0 by setting XTALCR[OSCOFF] = 1 and XTALCR[SE] = 1.

In this mode, the X1 clock passes through a buffer to the rest of the device. See the X1 Input Level Characteristics with an External Clock Source (Non-crystal) table for buffer input requirements.

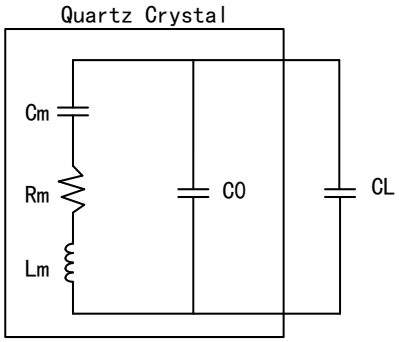
XTAL Output on XCLKOUT

Configure CLKSRCCTL3.XCLKOUTSEL and XCLKOUTDIVSEL.XCLKOUTDIV to route the electrical oscillator output to XCLKOUT for observation. See the GPIO Multiplexing Pins table for GPIOs supporting XCLKOUT.

5.7.3.4.2. Quartz Crystal

A quartz crystal can be electrically represented by an LCR (inductance-capacitance-resistance) circuit. Unlike a conventional LCR circuit, its low motional resistance gives it a very high Q factor and very low damping.

Figure 24 Crystal Electrical Equivalent



Note:

(1) Cm (motional capacitance): Represents crystal elasticity.

(2) Rm (motional resistance): Represents resistive losses in the crystal. It is not the equivalent crystal resistance, but can be approximated using the other crystal component values.

(3) Lm (motional inductance): Represents the vibrating mass of the crystal.

(4) C0 (shunt capacitance): Capacitance formed by the two crystal electrodes and stray package capacitance.

(5) CL (load capacitance): Effective capacitance seen at the crystal electrodes. External to the crystal, it pulls the crystal frequency. The frequency tolerance in ppm in crystal datasheets is usually associated with CL.

Consult the crystal manufacturer on the definition of CL to ensure correct values are used in calculations.

CL1 and CL2 are in series; use the series capacitance formula to calculate the equivalent total capacitance. Add stray PCB capacitance to this value.

Note: Both the electrical oscillator and crystal require load capacitance. Select values that satisfy both requirements.

5.7.3.4.3. GPIO Mode

X2 can serve as GPIO18, depending on the XTAL operating mode.

5.7.3.4.4. Normal Operation

ESR - Effective Series Resistance

Equivalent series resistance is the resistive load the crystal presents to the electrical oscillator at resonance. Higher ESR reduces the quality factor and the likelihood of starting or sustaining oscillation. The relationship between ESR and crystal components is shown below.

$$\mathrm{ESR} = Rm * (1 + \frac{C0}{CL})^2$$

Note: ESR differs from crystal motional resistance, but can be approximated by it when effective load capacitance is much greater than shunt capacitance.

Rneg (Negative Resistance)

Negative resistance is the impedance the electrical oscillator presents to the crystal, representing the energy it must supply to overcome oscillation losses.

Rneg describes a circuit that supplies rather than dissipates energy and can be regarded as overall circuit gain. To ensure crystal startup under all conditions, Rneg should exceed ESR by a factor of 3 to 5.

The negative resistance curves show variation with crystal components. Crystal shunt capacitance (C0) and effective load capacitance (CL) strongly affect oscillator negative resistance. See the Crystal Equivalent Series Resistance (ESR) Requirements table for design limits.

Startup Time

Crystal ESR and damping resistance (Rd) strongly affect startup time. Higher values increase startup time. A long startup time indicates a poor match between the crystal and circuit components.

See Crystal Oscillator Specifications for startup time. Actual startup time also depends on the crystal and external components.

DL (Drive Level)

Drive level is the power supplied by the electrical oscillator and dissipated by the crystal.

If actual drive exceeds the crystal's maximum drive level, add a damping resistor (Rd) to limit current and reduce crystal dissipation. Rd reduces circuit gain, so evaluate its actual value to ensure all other startup and sustained-oscillation conditions are met.

5.7.3.4.5. Selecting a Crystal

Refer to Crystal Oscillator Specifications:

（1） Select a crystal frequency (for example, 20MHz).

（2） Verify crystal ESR <= 50Ω, meeting the 20MHz specification.

（3） Verify the manufacturer's required load capacitance is between 6pF and 12pF, meeting the 20MHz specification.

CL1 and CL2 are in series. If CL1 = CL2, effective load capacitance CL = [CL1]/2.

Including board parasitics gives CL = [CL1]/2 + stray capacitance.

（4） Verify maximum crystal drive level >= 1mW. Otherwise, use damping resistor Rd. See DL - Drive Level for additional considerations when using Rd.

5.7.3.4.6. Testing

Consult the manufacturer for detailed crystal resonator parameters. Examples of parameter measurements follow:

Crystal circuits are highly sensitive to capacitance, so avoid connecting oscilloscope probes to X1 and X2. If monitoring X1/X2 is necessary, use an active probe with capacitance below 1pF.

- Frequency
  - Route XTAL to XCLKOUT.
  - Measure this frequency as the crystal frequency.
- Negative Resistance
  - Route XTAL to XCLKOUT.
  - Place a potentiometer in series with the crystal between the load capacitors.
  - Increase resistance until the XCLKOUT clock stops.
  - This resistance plus actual crystal ESR is the oscillator's negative resistance.
- Startup Time
  - Turn XTAL off.
  - Route XTAL to XCLKOUT.
  - Turn XTAL on and measure the time until XCLKOUT remains within a 45% to 55% duty cycle.

5.7.3.4.7. Common Issues and Debugging Tips

- Crystal Does Not Start
  - Review Selecting a Crystal and ensure all requirements are met.
- Crystal Takes a Long Time to Start
  - If Rd is fitted, its resistance is too high.
  - If no damping resistor is fitted, crystal ESR is too high or high load capacitance has reduced total circuit gain excessively.

5.7.3.4.8. Crystal Oscillator Specifications

Table 64 Crystal Oscillator Parameters

Symbol	Parameter	Min	Max	Unit

CL1/CL2	Load capacitance	12	24	pF
C0	Crystal shunt capacitance		7	pF

Table 65 Crystal Equivalent Series Resistance (ESR) Requirements

Crystal frequency (MHz)	Maximum ESR (Ω) (CL1 = CL2 = 12pF)	Maximum ESR (Ω) (CL1 = CL2 = 24pF)
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

Note:

(1) Crystal shunt capacitance (C0) must be less than or equal to 7pF.

(2) ESR = negative resistance/3

Table 66 Crystal Oscillator Electrical Characteristics

Parameter		Test conditions	Min	Typ	Max	Unit
Startup time (1)	f = 10MHz	Maximum ESR = 110Ω CL1 = CL2 = 24pF C0 = 7pF		8		ms
	f = 20 MHz	Maximum ESR = 50Ω CL1 = CL2 = 24pF C0 = 7pF		4		ms
Crystal drive level (DL)					1	mW

Note:

(1) Startup time depends on the crystal and oscillation circuit components.

5.7.3.5. Internal Oscillators

To reduce board cost and application development time, the device includes two independent internal oscillators, INTOSC1 and INTOSC2. Both are enabled at power-up by default. INTOSC2 is the system reference clock (OSCCLK) source and INTOSC1 is the backup. INTOSC1 can also be manually configured as the system reference clock (OSCCLK).

The following table provides internal oscillator electrical characteristics for evaluating whether the module meets application timing requirements.

Table 67 INTOSC Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit

f_{INTOSC}	Frequency, INTOSC1 and INTOSC2	All	9.7	10	10.3	MHz
$f_{INTOSC-STABILITY}$	Frequency stability at room temperature	30°C, nominal VDD		±0.3		%
	Frequency stability	All	–3		3	%
$t_{INT0SC-ST}$	Startup and settling time			15	20	μs

5.7.3.6. PLL

Table 68 PLL Power Consumption and Leakage

Mode	Conditions	Min	Typ	Max	Unit
Normal	0.9v/1V/1.1V -40℃/30℃/125℃	1.2	2	3	mA
Power-down			5	15	μA

Table 69 PLL Characteristics

Parameter	Description	Min	Typ	Max	Unit
f_{ref}	Reference frequency	2	10	20	MHz
N_{PLL}	Feedback divider ratio	6		127.75	
S_{fra}	Fractional step		0.25		
N_{PLL_OUT}	Output divider ratio	1		8	
T_{PLL}	Lock time	25.5μs+1024*tc(oscclk)			μs
F_{VCO}	VCO frequency, AVDD = 2.9 to 3.6, Tj = 40 to 125℃	100	/	400	MHz
f_{out}	PLL output frequency	15		200	MHz
f_{PLL_IN}	PLL clock duty cycle	45	-	55	%

5.7.4. Flash Parameters

Table 70 Minimum Flash Wait States at Different System Frequencies (FRDCNTL[RWAIT])

System frequency	RWAIT(1)
0<f≤36MHz	0
36MHz<f≤72MHz	1
72MHz<f≤108MHz	2
108MHz<f≤144MHz	3
144MHz<f≤180MHz	4
180MHz<f≤200MHz	5

Note:

(1) RWAIT: Number of Flash read wait states.

Table 71 Flash Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{pgh}	Programming wait time	20			ns
t_{prog}	Programming time		175		μs
t_{smp}	Programming time per pulse		TBD		μs
t_{erase1}	Page erase time at 10K-cycle endurance		TBD		ms
	Page erase time at 100K-cycle endurance		TBD		ms
t_{sme}	Erase time per pulse		TBD		μs
t_{me}	Mass erase time	20		150	ms
Endurance	All array		TBD		Period
	2 Mbits		TBD		Period
Read cycle time				25	ns
$t_{retention}$ data retention duration (T_J = 125℃)		10			Years

Note: Recommended operating conditions: T_A = -40℃ to 105℃, V_{DD} = 1.0V to 1.2V, V_{DDIO} = 3.1V to 3.6V, V_{SS} = 0V, C_{LOAD} = 0.01pf.

5.7.5. Debug and Emulation

G32R502x supports the following three emulation interfaces:

- JTAG
- cJTAG
- SWD

The JTAG port (IEEE 1149.1-1990 Standard Test Access Port and Boundary-Scan Architecture) has four dedicated pins: TMS, TDI, TDO, and TCK. The cJTAG port (IEEE 1149.7-2009 Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture) is a compact JTAG interface requiring only TMS and TCK, freeing traditional GPIO35 (TDI) and GPIO37 (TDO) for other multiplexed functions.

JTAG signals generally require no buffers when the MCU is within 6 inches (15.24cm) of the JTAG connector and no other device is in the chain. Otherwise, buffer each signal. Series resistors are generally unnecessary for 10MHz debug probe operation. For high emulation speeds around 35MHz, use a 22Ω series resistor on each JTAG signal.

Connect the JTAG debug probe connector's PD (power detect) terminal to the board's 3.3V supply. Connect GND and TDIS (cable disconnect sense) to board ground. Loop the connector TCK output back to RTCK input so the probe can detect clock continuity. This MCU does not support EMU0 and EMU1 on 14-pin and 20-pin emulation connectors. Pull these signals high at the connector with on-board 2.2kΩ to 4.7kΩ resistors, depending on debugger drive strength. 2.2kΩ is commonly used.

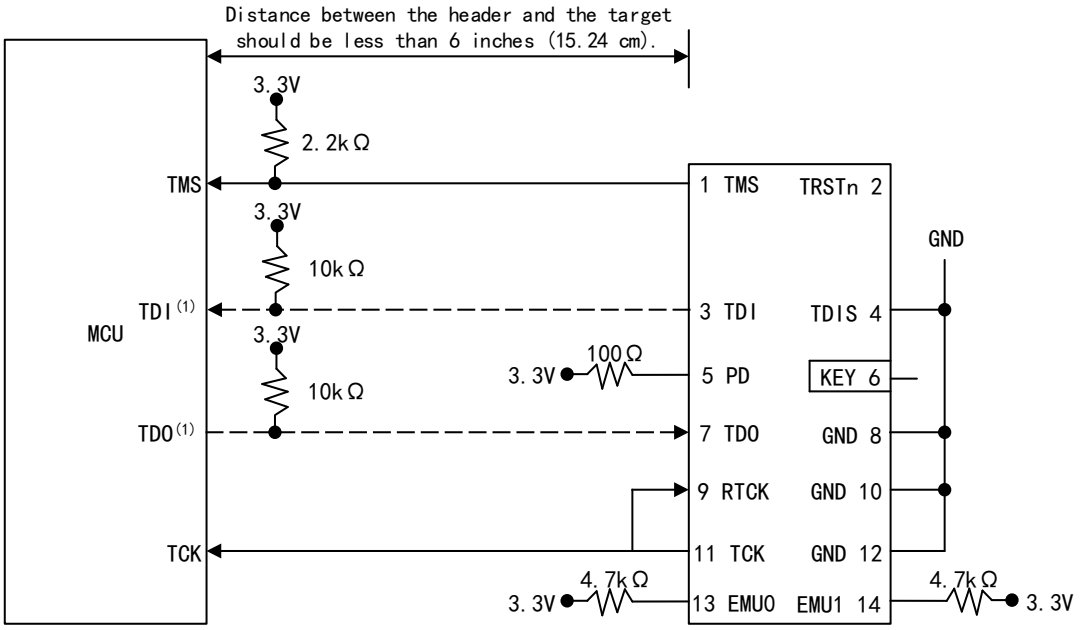
The connector reset terminal is an open-drain output from the JTAG debug probe connector for

resetting board components by probe command (20-pin connector only).

JTAG TDI is the default pin mux selection. The internal pull-up is disabled by default. When using JTAG TDI, enable the internal pull-up or add an external board pull-up to prevent a floating input. In cJTAG mode, this pin can be used as GPIO.

JTAG TDO is the default pin mux selection. The internal pull-up is disabled by default. When JTAG is inactive, TDO is in the high-impedance state and the pin floats. Enable the internal pull-up or add an external board pull-up to prevent a floating GPIO input. In cJTAG mode, this pin can be used as GPIO.

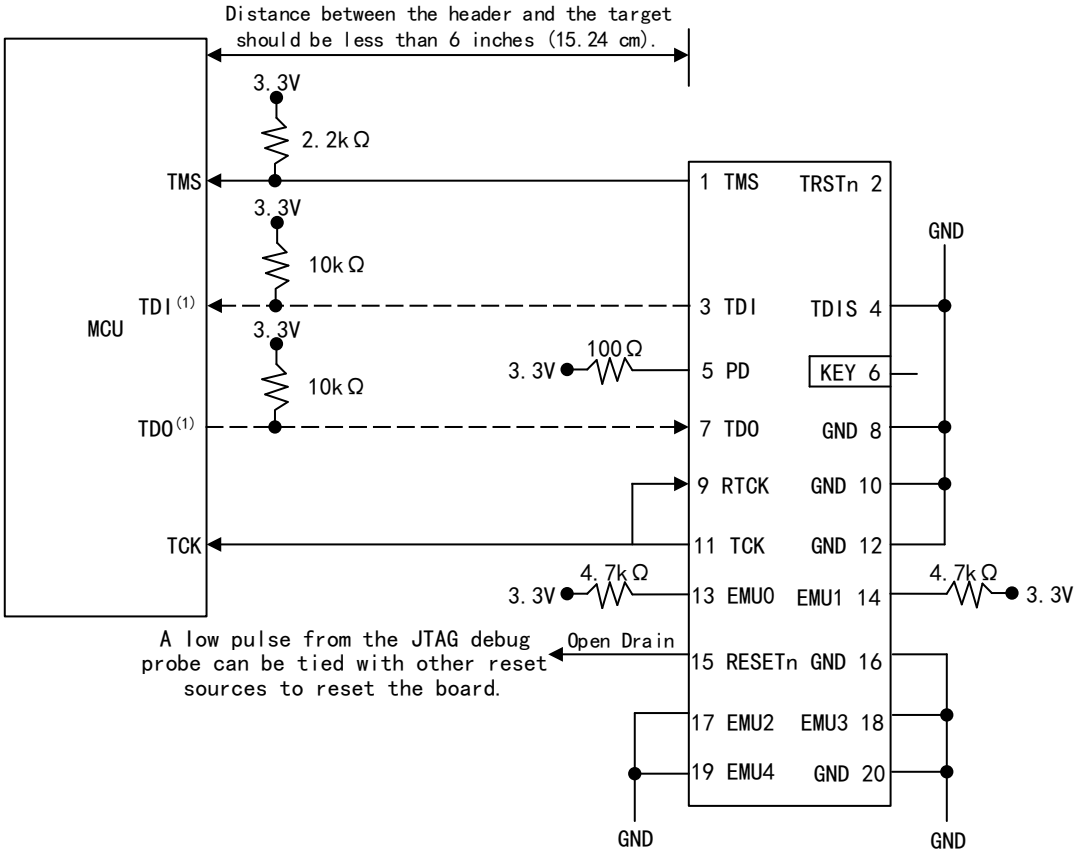
Figure 25 Connection to a 14-pin JTAG Connector



Note:

(1) cJTAG does not require TDI or TDO connections; these pins can be used as GPIO.

Figure 26 Connection to a 20-pin JTAG Connector



Note:

(1) cJTAG does not require TDI or TDO connections; these pins can be used as GPIO.

5.7.5.1. JTAG Electrical Data and Timing

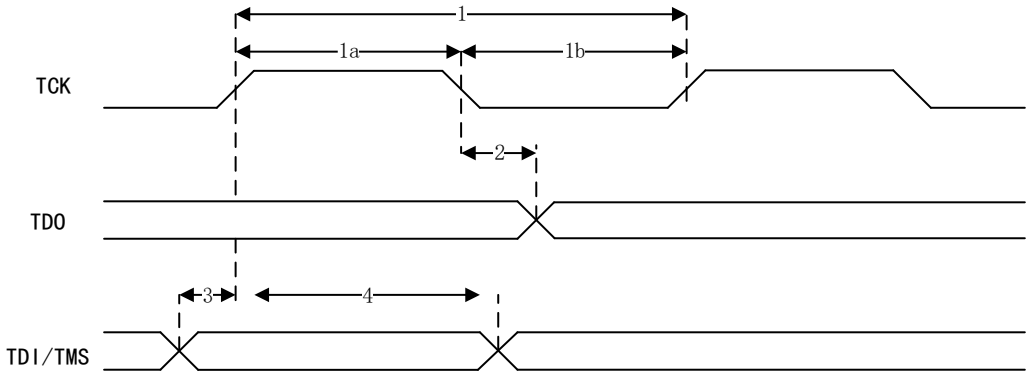
Table 72 JTAG Timing Requirements

No.	Symbol	Parameter	Min	Max	Unit
1	$t_{c(TCK)}$	Cycle time, TCK	66.66		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of tc)	26.66		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of tc)	26.66		ns
3	$t_{su(TDI-TCKH)}$	Input setup time, TDI valid to TCK high	13		ns
	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	13		
4	$t_{h(TCKH-TDI)}$	Input hold time, TCK high to TDI valid	7		ns
	$t_{h(TCKH-TMS)}$	Input hold time, TCK high to TMS valid	7		

Table 73 JTAG Switching Characteristics

No.	Symbol	Parameter	Min	Max	Unit
2	$t_{d(TCKL-TDO)}$	Delay time, TCK low to TDO valid	6	25	ns

Figure 27 JTAG Timing



5.7.5.2. cJTAG Electrical Data and Timing

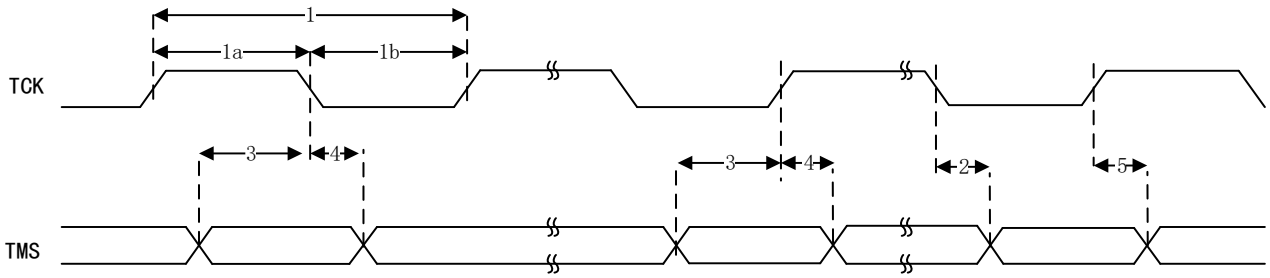
Table 74 cJTAG Timing Requirements

No.	Symbol	Parameter	Min	Max	Unit
1	$t_{c(TCK)}$	Cycle time, TCK	100		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of tc)	40		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of tc)	40		ns
3	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	15		ns
	$t_{su(TMS-TCKL)}$	Input setup time, TMS valid to TCK low	15		ns
4	$t_{h(TCKH-TMS)}$	Input hold time, CK high to TMS valid	2		ns
	$t_{h(TCKL-TMS)}$	Input hold time, TCK low to TMS valid	2		ns

Table 75 cJTAG Switching Characteristics

No.	Symbol	Parameter	Min	Max	Unit
2	$t_{d(TCKL-TMS)}$	Delay time, TCK low to TMS valid	6	20	ns
5	$t_{dis(TCKH-TMS)}$	Delay time, TCK high to TMS disabled		20	ns

Figure 28 cJTAG Timing Diagram



5.7.6. GPIO Electrical Data and Timing

Peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. At reset, GPIO pins are configured as inputs. For selected inputs, users can choose the number of qualification samples to filter unwanted noise.

The GPIO module includes the Output X-BAR, which routes internal signals to GPIO mux positions denoted OUTPUTXBARx. It also includes the Input X-BAR, which routes any GPIO input to IP blocks such as ADC, CAP, PWM, and external interrupts.

5.7.6.1. GPIO Output Timing

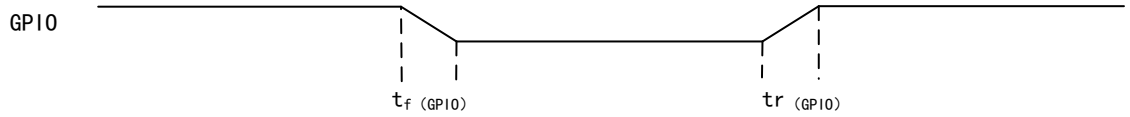
Table 76 General-Purpose Output Switching Characteristics

Symbol	Parameter	Min	Max	Unit
$t_{r(GPIO)}$	Rise time, GPIO low to high		8(1)	ns
$t_{f(GPIO)}$	Fall time, GPIO high to low		8(1)	ns
f_{GPIO}	Switching frequency		31.25	MHz

Note:

(1) Rise and fall times vary with load. Assume a 40pF load.

Figure 29 General-Purpose Output Timing



5.7.6.2. GPIO Input Timing

Table 77 General-Purpose Input Timing Requirements

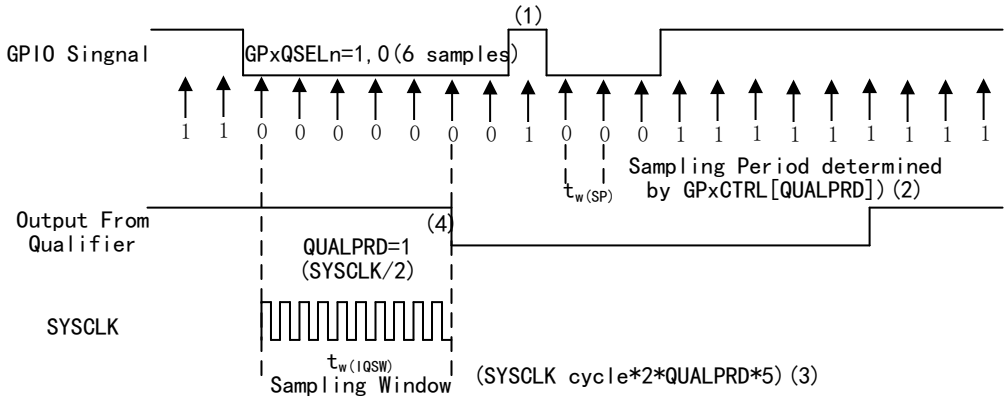
Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(SP)}$	Sampling period	QUALPRD=0	$1t_{c(SYSCLK)}$		Period
		QUALPRD≠0	$2t_{c(SYSCLK)}$*QUALPRD		
$t_{w(IQSW)}$	Input qualification sampling window		$t_{w(SP)}$*(n(1)-1)		Period
$t_{w(GPI)}$(2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SYSCLK)}$		Period
		With input qualification	$t_{w(IQSW)}$+ $t_{w(SP)}$+ $1t_{c(SYSCLK)}$		

Note:

(1) n is the number of qualification samples defined by GPxQSELn.

(2) For $t_{w(GPI)}$, measure pulse width from VIL to VIL for active-low signals and from VIH to VIH for active-high signals.

Figure 30 Sampling Mode



Note:

(1) Input qualification ignores this short glitch. QUALPRD specifies the qualification sampling period and ranges from 00 to 0xFF. If QUALPRD = 00, the period is 1 SYSCLK cycle. For any other value n, the period is 2n SYSCLK cycles, so the GPIO pin is sampled every 2n SYSCLK cycles.

(2) The qualification period selected through GPxCTRL applies to a group of 8 GPIO pins.

(3) Qualification uses 3 or 6 samples, as selected by GPxQSELn.

(4) In this example, the input must remain stable for at least 10 SYSCLK cycles for the qualification window to detect a change. That is, it must be stable for (5 × QUALPRD × 2) SYSCLK cycles, ensuring 5 sample periods for detection. Because the external signal is asynchronous, a pulse 13 SYSCLK cycles wide ensures reliable recognition.

5.7.6.3. Input Signal Sampling Window Width

The input sampling frequency relative to SYSCLK is:

- If QUALPRD ≠ 0, sampling frequency = SYSCLK/(2 × QUALPRD)
- If QUALPRD = 0, sampling frequency = SYSCLK

Within a sampling window, 3 or 6 samples determine signal validity, according to GPxQSELn. Based on General-Purpose Input Timing Requirements, window widths are calculated below, where $t_{c(SYSCLK)}$ is the SYSCLK period.

Two modes are available:

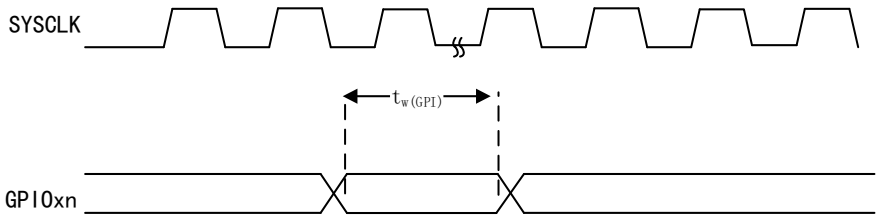
（1） When qualification uses 3 samples

- If QUALPRD ≠ 0, sampling window width = $2t_{c(SYSCLK)}$*QUALPRD*2
- If QUALPRD = 0, sampling window width = $t_{c(SYSCLK)}$*2

（2） When qualification uses 6 samples

- If QUALPRD ≠ 0, sampling window width = $2t_{c(SYSCLK)}$*QUALPRD*5
- If QUALPRD = 0, sampling window width = $t_{c(SYSCLK)}$*5

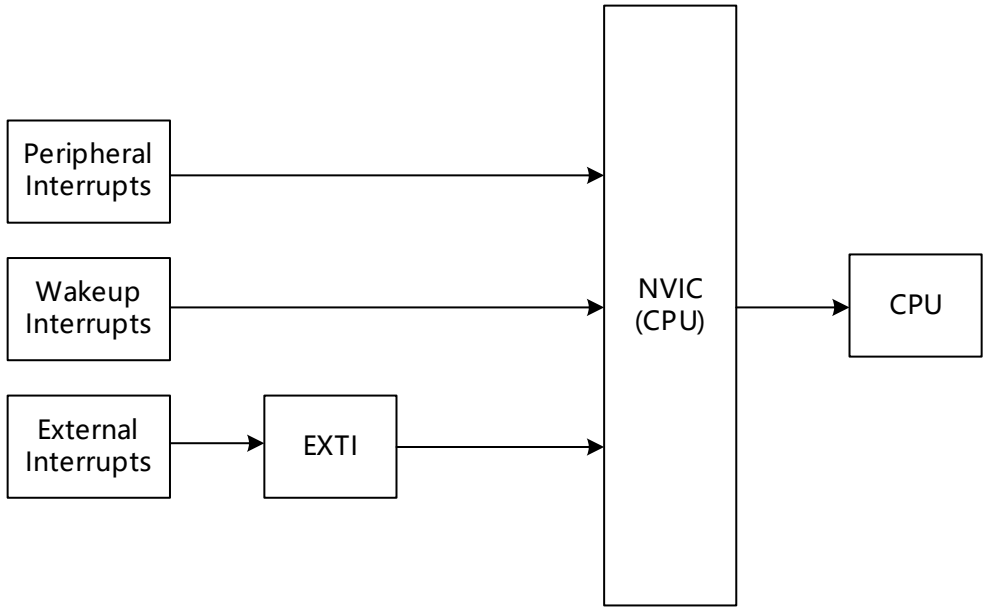
Figure 31 General-Purpose Input Timing



5.7.7. Interrupts (NVIC and EXTI)

The CPU supports interrupt numbers up to 226. All interrupts reach the CPU through NVIC. The external interrupt controller (EXTI) provides a total of 13 external (GPIO/INPUT_XBAR) and peripheral (COMP) interrupts.

Figure 32 Device Interrupt Architecture (EXTI)



5.7.7.1. External Interrupt (EXTI) Electrical Data and Timing

Table 78 External Interrupt Timing Requirements

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(INT)}$	Pulse duration, INT input low/high	Synchronous (1)	$2t_{c(SYSCLK)}$		Period
		With qualification (2)	$t_{w(IQSW)}+ t_{w(SP)}+ 1t_{c(SYSCLK)}$		

Note:

(1) INPUT_XBAR external inputs to EXTI support synchronous or asynchronous operation. GPIO and COMP signals to EXTI support only asynchronous triggering.

(2) See General-Purpose Input Timing Requirements for input qualification parameters.

Table 79 External Interrupt Switching Characteristics

Parameter (1)	Min	Max	Unit

$t_{d(INT)}$	Delay time, INT low/high to interrupt vector fetch (2)	Minimum time from interrupt assertion until the interrupt vector table appears on the address bus (3)	$t_{w(IQSW)}$+ $6t_{c(SYSCLK)}$		Period
		Minimum time from interrupt assertion until execution of the first ISR instruction (3)	$t_{w(IQSW)}$+ $18t_{c(SYSCLK)}$		Period

Note:

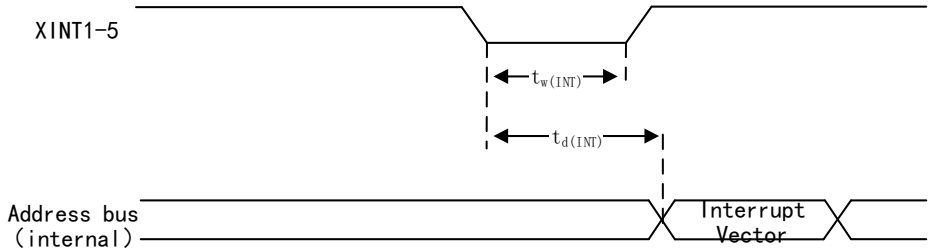
(1) See General-Purpose Input Timing Requirements for input qualification parameters.

(2) Assumes the ISR resides in single-cycle memory.

(3) Measured with no instruction fetch wait, no bus access wait, and no other interrupts.

(4) The CPU supports interrupt nesting and preemption, so a maximum cannot be estimated. The table provides minimum reference values without nesting, preemption, or bus waits.

Figure 33 External Interrupt Timing



5.8. Analog Peripherals

5.8.1. Analog Pins and Internal Connections

Table 80 Analog Pins and Internal Connections

Pin name	Pin/package				ADC		DAC	Comparator subsystem (mux)				AIO input/GPIO
	LQFP80	LQFP64	HTQFP48	VQFN32	A	C		High positive (HPMXSEL)	High negative (HNMXSEL)	Low positive (LPMXSEL)	Low negative (LNMXSEL)	
VREFHI	20	16	12	-(4)								
VREFLO	21	17	13	-(4)	A13	C13						
Analog group 1								COMP1				
A6	10	6	4(1)	2(1)	A6	-		2		2		GPIO228(3)
C9	13	9	6	4	-	C9		0		0		GPIO224(3)
C7	14	10	7(1)	5(1)	-	C7		3	0	3	0	AIO233
A11	16	12	8	6(1)	A11	-		1	1	1	1	AIO237
A1/DACB_OUT	18	14	10	7(1)	A1	-	DACB_OUT	4		4		AIO232
Analog group 2								COMP2				
A10/C10	29	25	21	13(1)	A10	C10		3	0	3	0	GPIO230(3)
Analog group 3								COMP3				
C6	11	7	4(1)	2(1)	-	C6		0		0		GPIO226(3)
A3/C5	12	8	5	3	A3	C5		3	0	3	0	GPIO242(3)
A14	15	11	7(1)	5(1)	A14	-		4		4		AIO239
A5/C2/VDAC	17	13	9	6(1)	A5	C2	VDAC	1	1	1	1	AIO244
A0/DACA_OUT	19	15	11	7(1)	A0	-	DACA_OUT	2		2		AIO231
Analog group 4								COMP4				
A7/C3	23	19	15	8(1)	A7	C3		1	1	1	1	AIO245
Combined analog group 2/4								COMP2/4				

Pin name	Pin/package				ADC		DAC	Comparator subsystem (mux)				AIO input/GPIO
	LQFP80	LQFP64	HTQFP48	VQFN32	A	C		High positive (HPMXSEL)	High negative (HNMXSEL)	Low positive (LPMXSEL)	Low negative (LNMXSEL)	
A12/C1	22	18	14	8(1)	A12	C1		COMP2: 1 COMP4: 2	1	COMP2: 1 COMP4 : 2	COMP2: 1	AIO238
A8/C11	24	20	16	9	A8	C11		COMP2: 4 COMP4 : 4		COMP2: 4 COMP4: 4		AIO241
A4/C14	27	23	19	12	A4	C14		COMP2: 0 COMP4: 3	COMP4: 0	COMP2: 0 COMP4: 3	COMP4: 0	AIO225
A9/C8	28	24	20	13(1)	A9	C8		COMP2: 2 COMP4: 0		COMP2: 2 COMP4: 0		GPIO227(3)
Other analog												
Temperature sensor (2)	-	-	-	-	-	C12		COMP2: 5				
A2	4	2	2	32	-	-						GPIO28(3)(5)
C0	33	27	22	-	-	-						GPIO20(3)
A15	34	28	-	-	-	-						GPIO21(3)
C4	35	29	23	-	-	-						GPIO13(3)
C15	36	30	24	-	-	-						GPIO12(3)

Note:

(1) This signal is bonded with another signal to a single pin in this package.

(2) Internal connection only; not connected to a device pin.

(3) GPIOs on these analog pins provide full digital input and output and are called AGPIOs. They are disconnected by default, with both analog and digital functions disabled. See Digital Inputs and Outputs on ADC Pins (AGPIO) for configuration details.

(4) On the VQFN32 package, VREFHI is internally connected to VDDA and VREFLO to VSSA.

(5) GPIO28 and comparator 4 (COMP4) cannot be used simultaneously.

Figure 34 Analog Subsystem Block Diagram

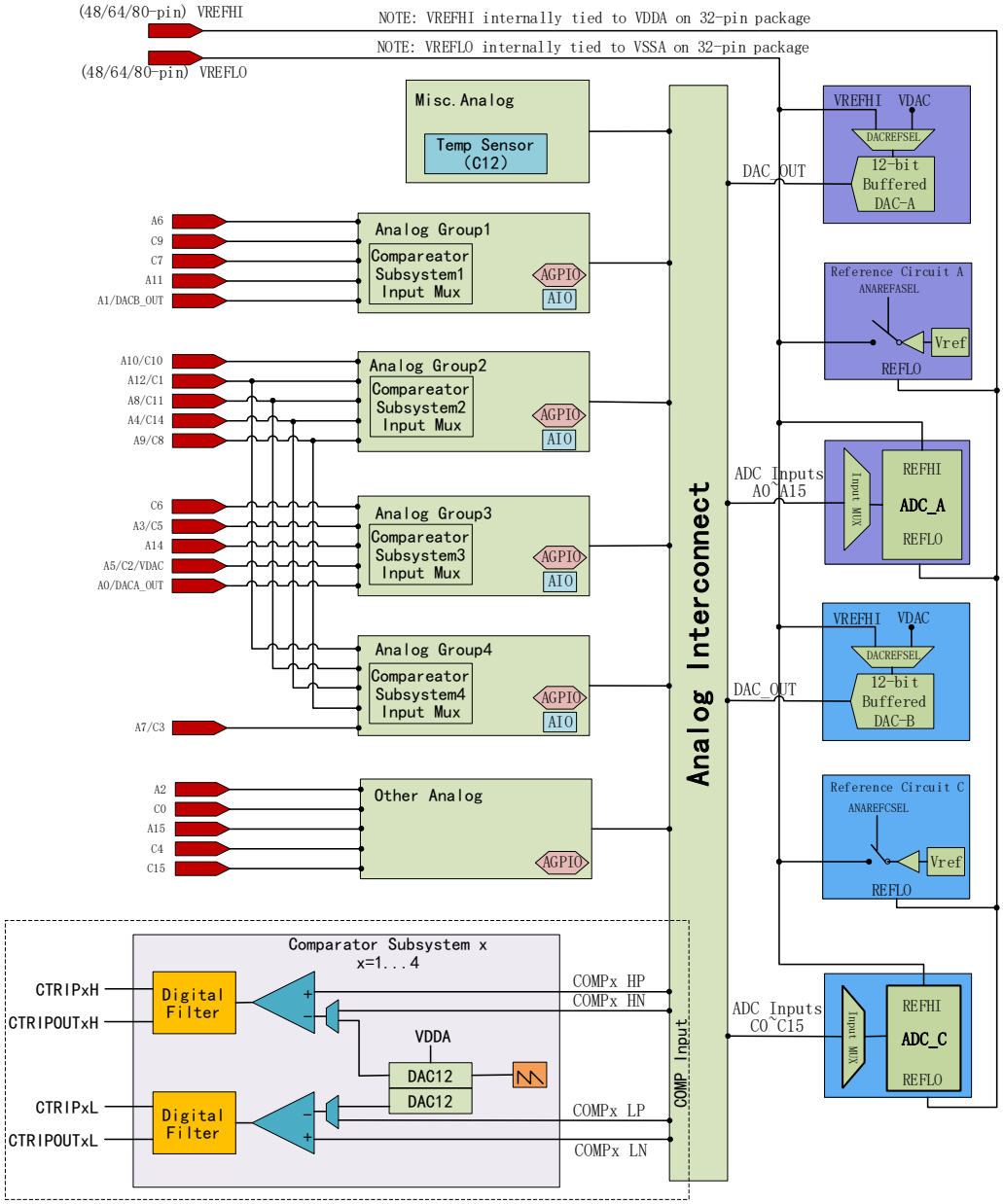
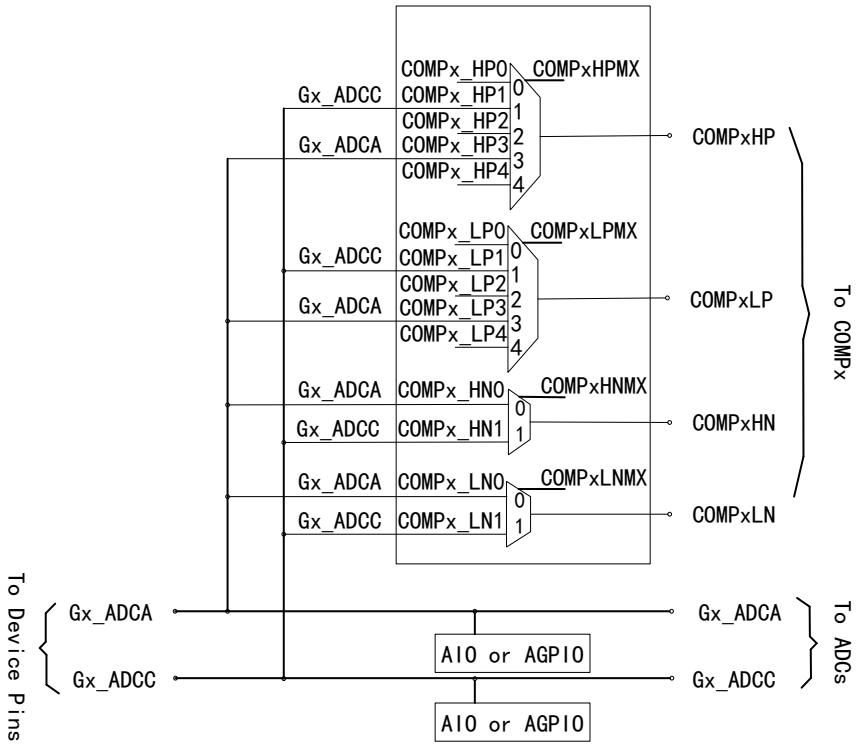


Figure 35 Analog Group Connections



5.8.2. Analog-to-Digital Converter (ADC)

The ADC is a 12-bit successive approximation register (SAR) converter. Its analog circuitry, called the core, includes the channel-selection mux, sample-and-hold (S/H) circuit, successive approximation circuit, voltage reference, and analog support circuits. The digital circuitry, called the wrapper, includes programmable conversion logic, result registers, analog circuit interface, peripheral bus interface, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module contains one sample-and-hold (S/H) circuit. Multiple instances on the same chip support simultaneous sampling or independent operation. The ADC wrapper is based on start-of-conversion (SOC); see SOC Operation in the Analog-to-Digital Converter (ADC) chapter of the product user manual.

5.8.2.1. ADC Electrical Data and Timing

Keep ADC inputs below VDDA + 0.3V. Above this level, an input may disturb other channels through two mechanisms:

- An overvoltage ADC input overdrives the COMP mux, disturbing all channels sharing that COMP mux. This persists whether or not the ADC samples the overvoltage input.
- Sampling an overvoltage input pulls VREFHI higher, disturbing subsequent conversions on any channel until VREF settles.

Keep VREFHI below VDDA + 0.3V for proper operation. Exceeding this level may activate the blocking circuit, allowing the internal VREFHI value to float to 0V and

causing incorrect ADC conversions.

5.8.2.2. ADC Operating Conditions

Table 81 ADC Operating Conditions

Parameter	Test conditions	Min	Typ	Max	Unit
ADCCLK (derived from AHBCLK) (1)		5		53.33	MHz
Sampling rate				3.72	MSPS
Sampling window duration (set by ACQPS and PERx.SYSCLK) (2)	With Rs of 50Ω or less	75			ns
VREFHI	External reference	2.4	2.5 or 3.0	VDDA	V
	VQFN32 package (4)	VDDA	VDDA	VDDA	V
VREFHI(3)	Internal reference = 3.3V range		1.65		V
	Internal reference = 2.5V range		2.5		V
VREFLO		VSSA	VSSA	VSSA	V
VREFHI - VREFLO	External reference	2.4		VDDA	V
Conversion range	Internal reference = 3.3V range	0		3.3	V
	Internal reference = 2.5 range	0		2.5	V
	External reference	VREFLO		VREFHI	V

Note:

(1) ADC operating clock ≤ 50MHz when using the internal 3.3V reference

(2) The sampling window must also be at least 1 ADCCLK cycle long for correct ADC operation.

(3) In internal reference mode, the device drives the reference voltage onto VREFHI. Do not drive an external voltage onto this pin in this mode.

(4) On the VQFN32 package, VREFHI is internally connected to VDDA and VREFLO to VSSA. Internal reference mode is not supported.

Keep ADC inputs below VDDA + 0.3V. Above this threshold, the internal VREF may be disturbed, affecting other ADC or DAC results using the same VREF. Also keep VREFHI below VDDA + 0.3V. Exceeding this threshold may activate the blocking circuit, allowing internal VREFHI to float to 0V and causing incorrect ADC conversions or DAC outputs.

Table 82 General Characteristics

Parameter	Test conditions	Min	Typ	Max	Unit
ADCCLK conversion cycles	160MHz AHBCLK	10.1		11	ADCCLK
Power-up time	External reference mode			500	μs
	Internal reference mode			5000	μs
	Internal reference mode when switching between 2.5V and 3.3V ranges			5000	μs
VREFHI input current (1)			160		μA
Internal reference capacitance (2)		2.2			μF
External reference capacitance (2)		2.2			μF

Note:

(1) When an ADC input exceeds VDDA, VREFHI load current increases, causing inaccurate conversion.

(2) Ceramic capacitors in 0805 or smaller packages are preferred. Tolerance up to ±20% is acceptable.

Table 83 DC Characteristics

Parameter	Test conditions	Min	Typ	Max	Unit
Gain error	Internal reference voltage	-45		45	LSB
	External reference		±3		
Offset voltage error			±2		
Channel-to-channel gain error			±2		
Channel-to-channel offset voltage error			±2		
ADC-to-ADC gain error	Identical VREFHI and VREFLO for all ADCs		±3		
ADC-to-ADC offset voltage error	Identical VREFHI and VREFLO for all ADCs		±2		
DNL error	ADCCLK＞50MHz Except internal 3.3V reference	-1	±0.5	1	

Parameter	Test conditions	Min	Typ	Max	Unit
	ADCCLK≤50MHz All reference voltages				
INL error	ADCCLK＞50MHz Except internal 3.3V reference	-2	±1.0	2	
	ADCCLK≤50MHz All reference voltages				
ADC-to-ADC isolation	VREFHI = 2.5V, synchronous ADCs	-1.5		1.5	
	VREFHI = 2.5V, asynchronous ADCs	Not supported			

Table 84 AC Characteristics

Parameter	Test conditions	Min	Typ	Max	Unit
SNR(1)	VREFHI = 2.5V, fin = 100kHz, SYSCLK from X1, ADCCLK = 50MHz, Cache enabled		65.5		dB
	VREFHI = 2.5V, fin = 100kHz, SYSCLK from INTOSC, ADC CLK = 50MHz		58.0		
THD(1)	VREFHI = 2.5V, fin = 100kHz, ADCCLK = 50MHz, Cache enabled		74.9		dB
SFDR(1)	VREFHI = 2.5V, fin = 100kHz, ADCCLK = 50MHz, Cache enabled		74.1		dB
SINAD(1)	VREFHI = 2.5V, fin = 100kHz, SYSCLK from X1, ADC CLK = 50MHz, Cache enabled		64.9		dB
	VREFHI = 2.5V, fin = 100kHz, SYSCLK from INTOSC, Cache enabled		57.9		dB
ENOB(1)	VREFHI = 2.5V, fin = 100kHz, SYSCLK from X1, single ADC, ADCCLK = 50MHz, Cache enabled		10.5		Bit
	VREFHI = 2.5V, fin = 100kHz, SYSCLK from X1, synchronous ADCs, ADCCLK = 50MHz, Cache enabled		10.5		
	VREFHI = 2.5V, fin = 100kHz, SYSCLK from X1, asynchronous ADCs, ADCCLK = 50MHz		Not supported		
PSRR	VDD = 1.1V DC + 100mV DC-to-sine (at 1kHz), ADCCLK = 50MHz		58		dB
	VDD = 1.1V DC + 100mV DC-to-sine (at 300kHz), ADCCLK = 50MHz		57		

Parameter	Test conditions	Min	Typ	Max	Unit
	VDDA = 3.3V DC + 200mV DC-to-sine (at 1kHz), ADCCLK = 50MHz		58		
	VDDA = 3.3V DC + 200mV Sine (at 900kHz), ADCCLK = 50MHz		57		

Note:

(1) I/O activity on pins adjacent to ADC inputs and VREFHI was minimized as a best practice to reduce capacitive coupling and crosstalk.

(2) The effect of DC/DC regulator noise on the ADC depends strongly on PCB layout.

5.8.2.3. ADC Input Model

Table 85 ADC Input Characteristics

Symbol	Parameter	Reference mode	Value
Cp	Parasitic input capacitance	All	See the following table
Ron	Sampling switch resistance	External reference, 2.5V internal reference	500Ω
		3.3V internal reference	860Ω
Ch	Sampling capacitor	External reference, 2.5V internal reference	12.5pF
		3.3V internal reference	7.5pF
Rs	Nominal source impedance	All	50Ω

In single-ended operation, use this input model with the actual source impedance to determine sampling window duration.

Figure 36 Single-ended Input Model

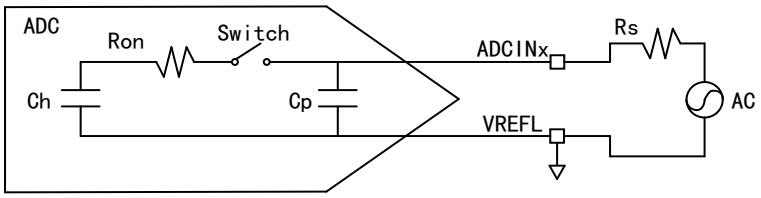


Table 86 Parasitic Capacitance per Channel

ADC channel	C_{p}(pF)	
	Comparator disabled	Comparator enabled
ADCINA0	-	-
ADCINA1	-	-
ADCINA2	-	-
ADCINA3	-	-

ADC channel	$C_{p(}$pF)	
	Comparator disabled	Comparator enabled
ADCINA4	-	-
ADCINA5	-	-
ADCINA6	-	-
ADCINA7	-	-
ADCINA8	-	-
ADCINA9	-	-
ADCINA14	-	-
ADCINA16	-	-
ADCINA17	-	-
ADCINA18	-	-
ADCINA19	-	-
ADCINA20	-	-
ADCAVREFHFB	-	-
ADCINC0	-	-
ADCINC4	-	-
ADCINC6	-	-
ADCINC13	-	-
ADCINC16	-	-
ADCINC17	-	-
ADCINC19	-	-
ADCCVREFFB	-	-

5.8.2.4. ADC Timing Diagram

The following figure shows conversion timing for two SOCs under these assumptions:

- SOC0 and SOC1 use the same trigger.
- No other SOC is converting or pending when the trigger occurs.
- The round-robin pointer is positioned so SOC0 converts first.
- ADCINTSEL is configured to set ADCINT at the end of SOC0 conversion. Whether this flag propagates to the CPU to cause an interrupt depends on NVIC configuration.

Figure 37 ADC Timing

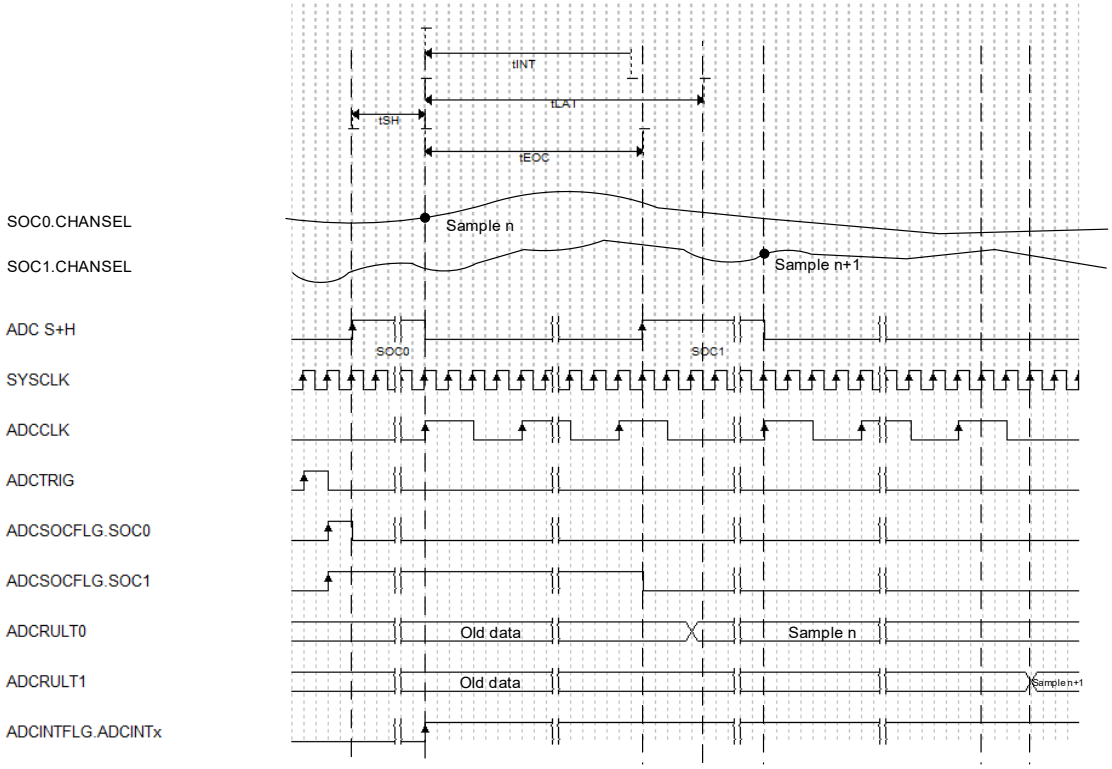


Table 87 ADC Timing Parameters

Parameter	Description
t_{SH}	S+H window duration. At the end of this window, the S+H capacitor voltage is the voltage to be digitized. Duration is (ACQPS + 1) SYSCLK cycles. ACQPS is independently configurable for each SOC, so tSH can differ among SOCs. Note: Regardless of device clock settings, the S+H capacitor value is captured approximately 5ns before the window ends.
t_{LAT}	Time from the end of the S+H window until the result is latched into ADCRESULTx. Reading ADCRESULTx before this time returns the previous conversion result.
t_{EOC}	Time from the end of the S+H window until the next conversion's S+H window can start. Subsequent sampling can begin before the result is latched.
t_{INT}	Time from the end of the S+H window until ADCINT is set, if configured. If INTPULSEPOS in ADCCTL1 is set, tINT coincides with end-of-conversion (EOC). If INTPULSEPOS is 0, tINT coincides with the end of the S+H window. If tINT triggers a result read through an ISR, ensure the read occurs after the result is latched; otherwise, the previous result is read. If INTPULSEPOS is 0 and OFFSET in ADCINTCYCLE is nonzero, setting ADCINT is delayed by OFFSET SYSCLK cycles. This delay can allow ISR entry when the sample is ready.

Table 88 ADC Timing in 12-bit Mode

ADCCLK prescaler		AHBCLK cycles				ADCCLK cycles
Prescaler ratio	PRESCALE	t_{LAT}	t_{EOC}	t_{INT} (early) (1)	t_{INT} (late)	t_{EOC}

ADCCLK prescaler		AHBCLK cycles				ADCCLK cycles
1	0	13	11	1	11	11
2	2	23	21	1	21	10.5
3	4	34	31	1	31	10.3
4	6	44	41	1	41	10.3
5	8	55	51	1	51	10.2
6	10	65	61	1	61	10.2
7	12	76	71	1	71	10.1
8	14	86	81	1	81	10.1

Note: The ADC open/short-circuit detection pull-up and pull-down resistors are changed to 5K and 7K.

(1) By default, when INTPULSEPOS is 0, t_{INT} occurs within one SYSCLK cycle after the S+H window. Change this through OFFSET in ADCINTCYCLE.

5.8.3. Temperature Sensor

5.8.3.1. Temperature Sensor Electrical Data and Timing

The temperature sensor measures device junction temperature. It is sampled through an internal ADC connection, and the value is converted to temperature using Geehy's software interface. When sampling it, the ADC must meet the acquisition time in Temperature Sensor Characteristics.

5.8.3.2. Temperature Sensor Characteristics

Measured under recommended operating conditions, unless otherwise specified

Table 89 Temperature Sensor Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Tacc	Temperature accuracy	External reference		±15		℃
$t_{startup}$	Startup time (TSNSCTL[ENABLE] to temperature sensor sampling)			500		μs
t_{SH}	ADC sample-and-hold time		450			ns

The internal sensor measures device junction temperature. Its output can be sampled through an internal ADC channel.

5.8.4. Buffered Digital-to-Analog Converter (DAC)

The buffered DAC comprises an internal 12-bit DAC and an analog output buffer capable of driving external loads. For loads above the typical value, a tradeoff can be made between load and output voltage swing.

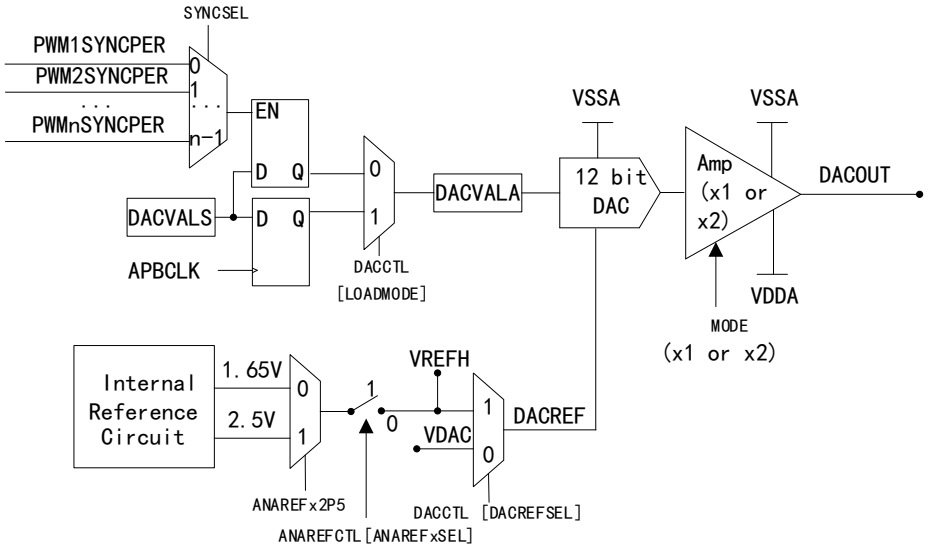
The general-purpose buffered DAC generates DC voltages or AC waveforms

such as sine, square, and triangle waves. Software writes to the DAC value register can take effect immediately or synchronize with PWMSYNCPER.

Each buffered DAC provides:

- 12-bit resolution
- Selectable reference voltage source
- X1 and X2 gain modes when using internal VREFHI
- Synchronization with PWMSYNCPER

Figure 38 Buffered DAC Block Diagram



Note: Add the VDAC reference voltage pin to the I/O information.

5.8.4.1. Buffered DAC Electrical Data and Timing

5.8.4.1.1. Buffered DAC Operating Conditions

Table 90 Buffered DAC Operating Conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
RL	Resistive load (1)		5			kΩ
CL	Capacitive load				100	pF
V-OUT	Valid output voltage range (2)	RL = 5kΩ	0.3		VDDA – 0.3	V
		RL = 1kΩ	0.6		VDDA – 0.6	V
Reference voltage (3)		VDAC or VREFHI	2.4	2.5 or 3.0	VDDA	V

Note: Typical values are measured at VREFHI = 3.3V and VREFLO = 0V; minimum and maximum values at VREFHI = 2.5V and VREFLO = 0V.

(1) The DAC can drive resistive loads down to 1kΩ, with a restricted output range.

(2) VOUT is the linear DAC output range. Voltages outside this range can be generated, but are nonlinear due to the buffer.

(3) For best PSRR, keep VDAC or VREFHI below VDDA.

5.8.4.1.2. Buffered DAC Electrical Characteristics

Table 91 General Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
	Resolution			12		Bit
	Load regulation		-0.5		0.5	mV/V
	Glitch impulse energy			0.5		V-ns
	Full-scale voltage output settling time	Settling to 2LSB after switching from 0.3V to 3V			2	μs
	Quarter-scale voltage output settling time	Settling to 2LSB after switching from 0.3V to 0.75V			1	μs
	Voltage output slew rate	Slew rate for transition from 0.3V to 3V	7.4		15.5	V/μs
	Load transient settling time (1)	5kΩ load			350	ns
		1kΩ load			557	ns
	Reference input resistance (2)	VDAC or VREFHI	160	200	240	kΩ
TPU	Power-up time	External reference mode			500	μs
		Internal reference mode			5000	μs

Note: Typical values are measured at VREFHI = 3.3V and VREFLO = 0V; minimum and maximum values at VREFHI = 2.5V and VREFLO = 0V.

(1) Settles within 3LSB.

(2) Per active buffered DAC module.

Table 92 DC Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
	Offset error	Midpoint	-8		8	mV
Gain	Gain error (1)		-2.5		2.5	Percentage of FSR
DNL	Differential nonlinearity (2)	Endpoint-corrected	-1	±0.5	1	LSB
INL	Integral nonlinearity	Endpoint-corrected	-5	±2.5	5	LSB

Note:

(1) Gain error is calculated over the linear output range.

(2) The DAC output is monotonic.

Table 93 AC Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
	Output noise	Integrated noise from 100Hz to 100kHz		600		μVrms
		Noise density at 10kHz		800		nVrms/√Hz
SNR	Signal-to-noise ratio	2.34375kHz，200KSPS		67.6		dB
THD	Total harmonic distortion	2.34375kHz，200KSPS		-71.3		dB
SFDR	Spurious-free dynamic range	2.34375kHz，200KSPS		80.3		dB
SINAD	Signal-to-noise-and-distortion ratio	2.34375kHz，200KSPS		66.1		dB
PSRR	Power supply rejection ratio (1)	DC		70		dB
		100kHz		30		dB

Note:

(1) VREFHI = 3.2V, VDDA = 3.3V DC + 100mV (sine)

Keep VDAC below VDDA + 0.3V for proper operation. Exceeding this level may activate the blocking circuit, allowing internal VDAC to float to 0V and causing incorrect DAC output. Also keep VREFHI below VDDA + 0.3V. Exceeding this level may activate the blocking circuit, allowing internal VREFHI to float to 0V and causing incorrect ADC conversions or DAC outputs.

5.8.4.1.3. Buffered DAC Diagrams

Figure 39 Buffered DAC Offset

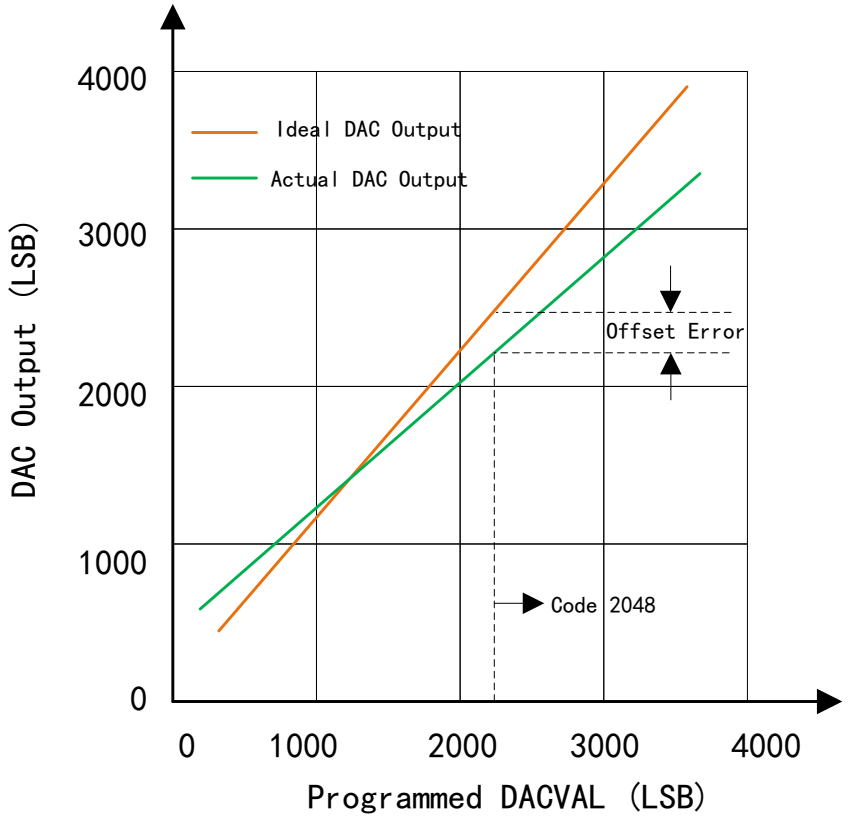


Figure 40 Buffered DAC Gain

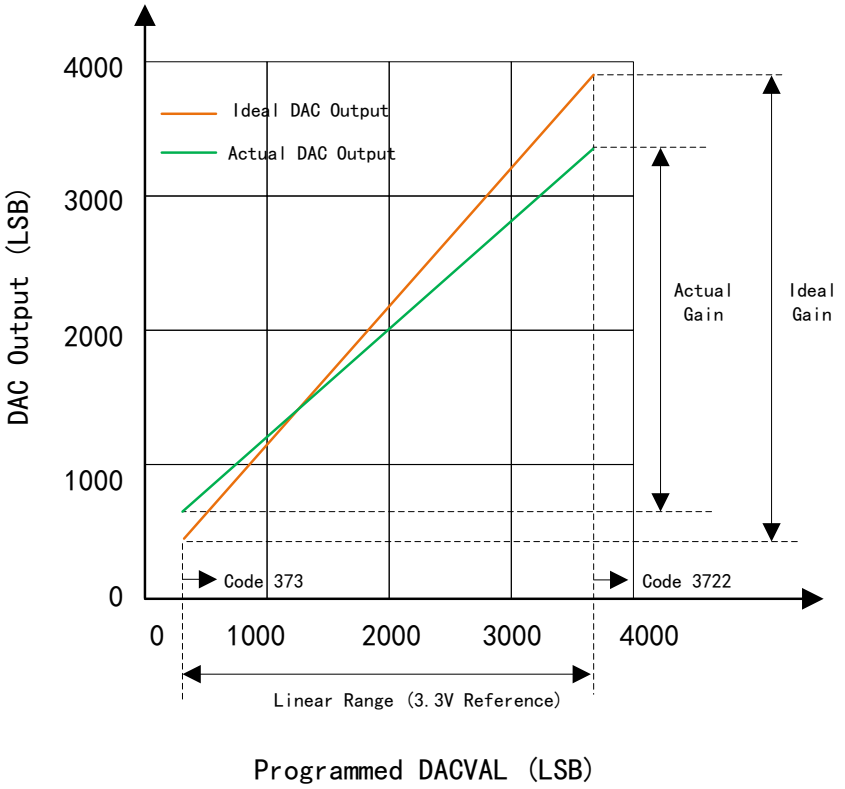
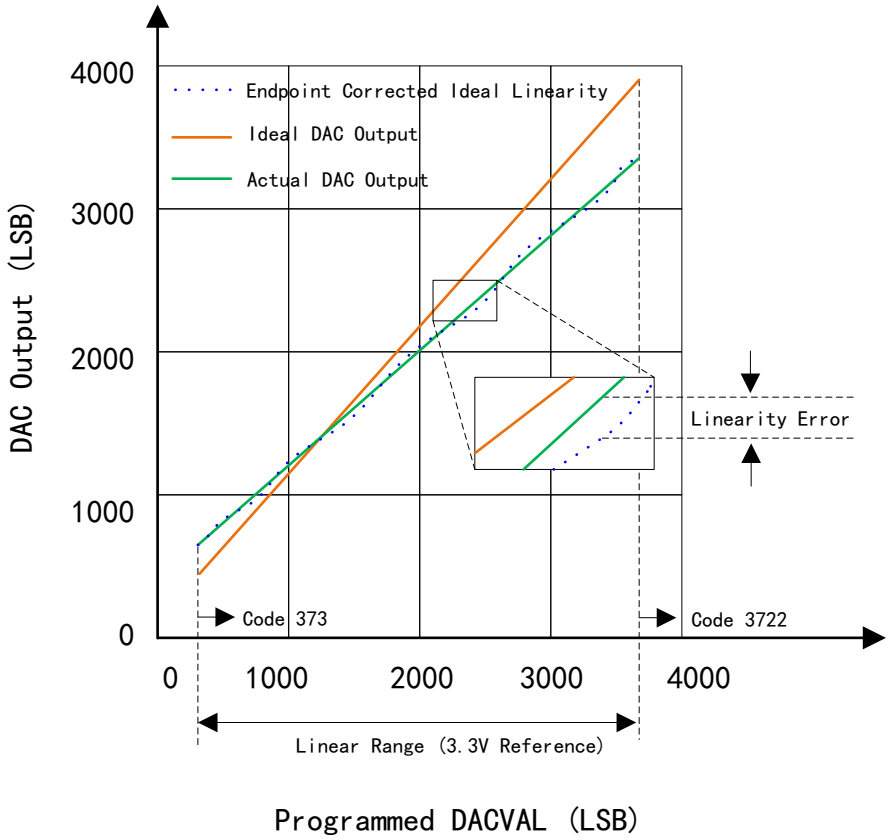


Figure 41 Buffered DAC Linearity



5.8.5. Comparator (COMP)

5.8.5.1. Main Features

The comparator subsystem (COMP) comprises analog comparators and supporting circuits useful for peak-current-mode control, switch-mode power supplies, power factor correction, voltage trip monitoring, and other power applications.

The comparator subsystem comprises multiple modules. Each contains two comparators, two 12-bit reference DACs, two digital filters, and one ramp generator. H denotes the high comparator and L the low comparator. Each generates a digital output indicating whether the positive input voltage exceeds the negative input. The positive input is driven by an external pin; see the Analog Subsystem chapter of the G32R502 Real-Time Microcontroller Technical Reference Manual for COMP mux options. The negative input can be driven by an external pin or programmable 12-bit reference DAC. Each output passes through a programmable digital filter that removes spurious transitions. Unfiltered output is also available. The ramp generator controls the high comparator's 12-bit reference DAC value.

5.8.5.1.1. COMP Comparator Electrical Characteristics

Measured under recommended operating conditions, unless otherwise specified

Table 94 COMP Comparator Electrical Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
TPU	Power-up time				500	μs
	Comparator input (COMPINxx) range		0		VDDA	V
	Input-referred offset error	Low common mode, inverting input set to 50mV	-20		20	mV
	Hysteresis (1)	1x		14		LSB
		2x		28		
		3x		43		
		4x		58		
	Response time (COMPINx change to PWM X-BAR or Output X-BAR output)	Step response		21	60	ns
		Ramp response (1.65V/μs)		26		
		Ramp response (8.25mV/μs)		50		ns
PSRR	Power supply rejection ratio	Up to 250kHz		46		dB
CMRR	Common-mode rejection		40			dB

	ratio					

Note:

(1) COMP DAC is the reference for the applied hysteresis, so hysteresis varies with COMP DAC reference voltage. Hysteresis applies to all comparator input source configurations.

Figure 42 COMP Comparator Input-Referred Offset

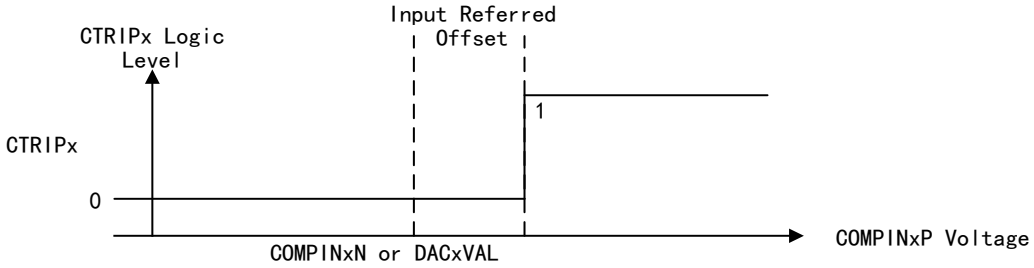
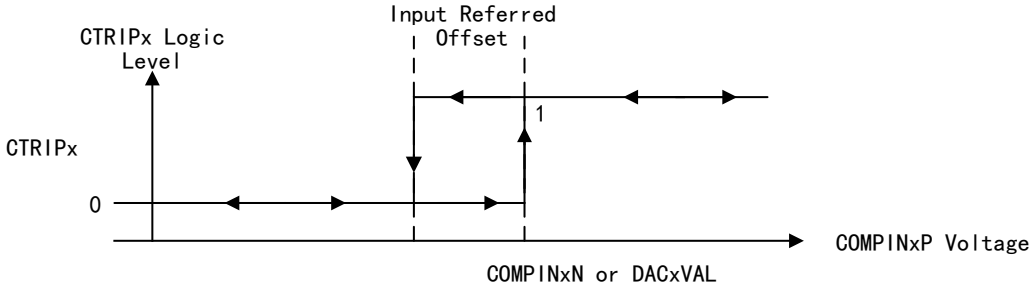


Figure 43 COMP Comparator Hysteresis



Measured under recommended operating conditions, unless otherwise specified

Table 95 COMP DAC Static Electrical Characteristics

Parameter	Test conditions	Min	Typ	Max	Unit
COMP DAC output range	Internal reference	0		VDDA	V
Static offset error (1)		-25		25	mV
Static gain error (1)		-2		2	Percentage of FSR
Static DNL	Endpoint-corrected	>-1		4	LSB
Static INL	Endpoint-corrected	-16		16	LSB
Settling time	Settling to 1LSB after a full-scale output change			1	μs
Resolution			12		Bit
COMP DAC output disturbance (2)	Error caused by comparator tripping or a COMP DAC code change in the same COMP module	-100		100	LSB
COMP DAC disturbance time (2)				200	ns

Note:

(1) Includes comparator input-referred error.

(2) A disturbance error may exist on COMP DAC output for a period after comparator tripping.

5.8.5.1.2. COMP Diagrams

Figure 44 COMP DAC Static Offset

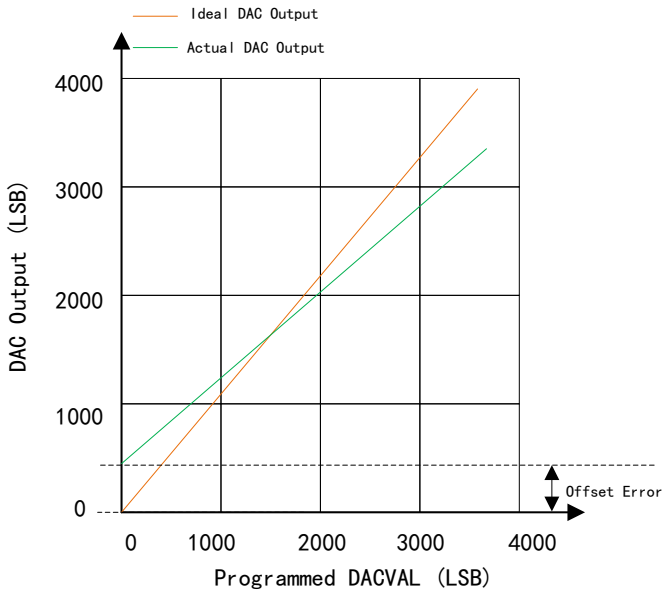


Figure 45 COMP DAC Static Gain

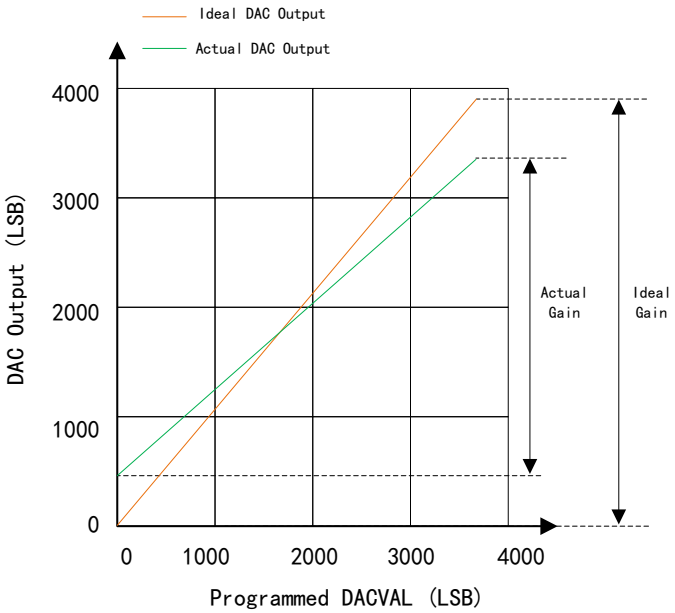
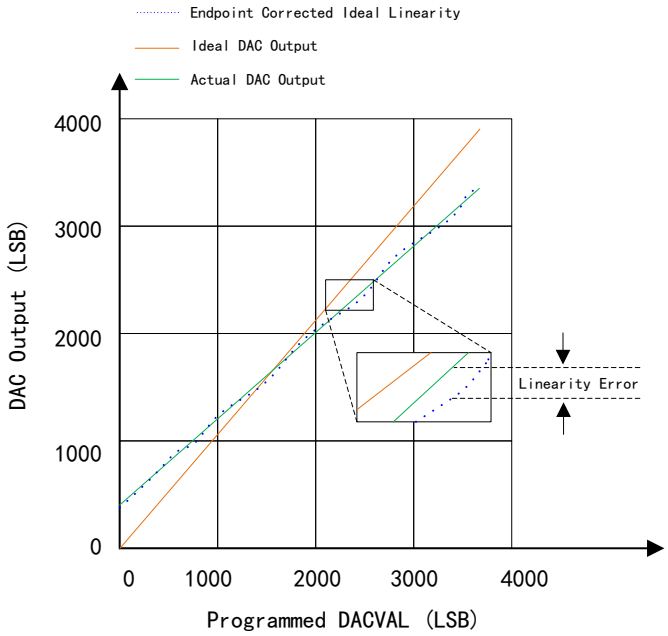


Figure 46 COMP DAC Static Linearity



5.9. Control Peripherals

5.9.1. Capture (CAP)

CAP provides precise timing of external events. It decodes voltage or current magnitude from duty-cycle-encoded sensors, measures pulse-train duty cycle and period and elapsed time between position sensor pulses, and measures rotational speed using, for example, a toothed sprocket sensed by a Hall sensor.

5.9.1.1. CAP Electrical Characteristics and Timing

Table 96 CAP Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SCO)}$			ns
		Synchronous	$2t_{c(SCO)}$			
		With input qualification	$1t_{c(SCO)}+ t_{w_(QSW)}$			

Table 97 CAP Switching Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20			ns

Note on interrupts: Due to CPU interrupt handling characteristics, do not use a system-level Clear Pending statement in a CAP ISR. At high capture frequencies, this statement may prevent subsequent interrupt entry. Omitting it avoids this issue.

5.9.2. Pulse Width Modulator (PWM)

PWM is a key peripheral for controlling power electronics in commercial and industrial equipment. The Type 4 PWM module generates complex pulse-width waveforms with minimal CPU overhead. Features include complex waveform generation, dead-band generation, flexible synchronization, advanced trip-zone functions, and global register reload.

5.9.2.1. PWM Electrical Characteristics and Timing

Table 98 PWM Timing Requirements

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(SYNCIN)}$	Synchronization input pulse width	Asynchronous	$2t_{c(PWMCLK)}$		Period
		Synchronous	$2t_{c(PWMCLK)}$)		
		With input qualification (1)	$1t_{c(PWMCLK)}$+ $t_{w(IQSW)}$		

Note:

(1) See General-Purpose Input Timing Requirements for input qualification parameters.

Table 99 PWM Switching Characteristics

Measured under recommended operating conditions, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
$t_{w(PWM)}$	Pulse duration, PWMx output high/low	20		ns
$t_{w(SYNCOUT)}$	Synchronization output pulse width	$8t_{c(SYSCLK)}$		Period
$t_{d(TZ-PWM)}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM high impedance		25	ns

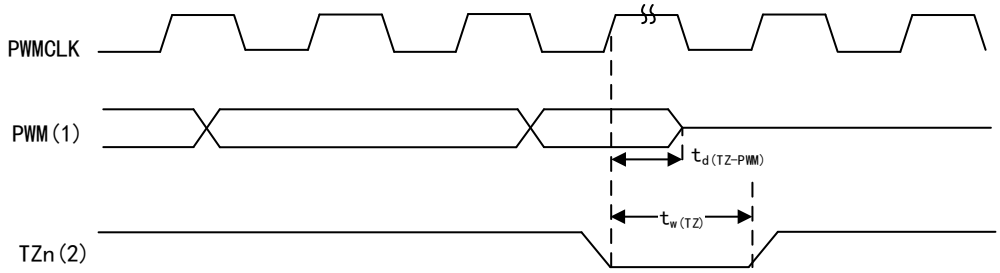
Table 100 Trip-Zone Input Timing Requirements

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(TZ)}$	Pulse duration, TZxn input low	Asynchronous	$1t_{c(PWMCLK)}$		Period
		Synchronous	$2t_{c(PWMCLK)}$		
		With input qualification (1)	$1t_{c(PWMCLK)}$+ $t_{w(IQSW)}$		

Note:

(1) See General-Purpose Input Timing Requirements for input qualification parameters.

Figure 47 PWM Hi-Z Characteristics



Note:

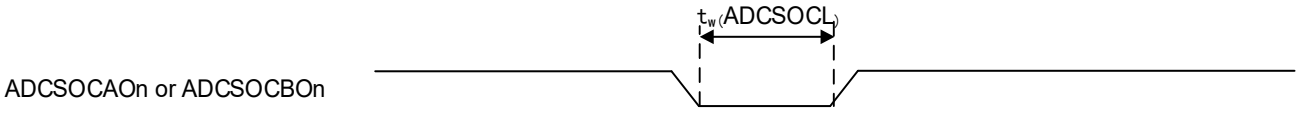
(1) PWM refers to all device PWM pins. After TZn goes high, PWM pin states depend on the PWM recovery software.

(2) TZn: TZ1n, TZ2n, TZ3n, TRIP1 to TRIP12

Table 101 External ADC Start-of-Conversion Switching Characteristics

Symbol	Parameter	Min	Max	Unit
$t_{w(ADCSOCL)}$	Pulse duration, ADCSOCxOn low	$32t_{c(SYSCLK)}$		Period

Figure 48 ADCSOCAO or ADCSOCBO Timing

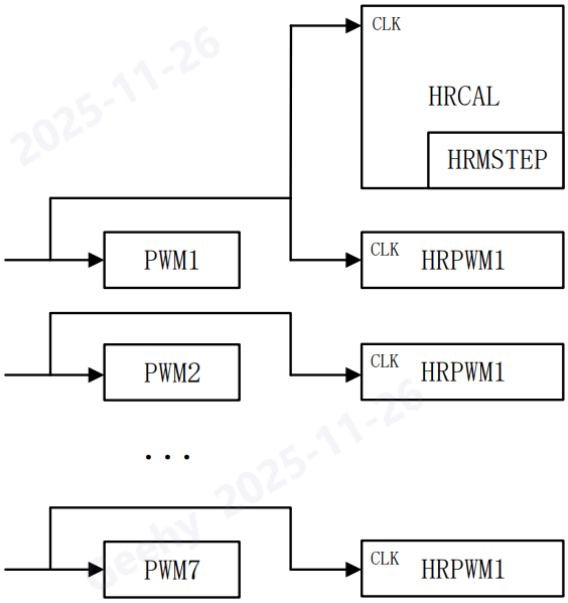


5.9.3. High-Resolution Pulse Width Modulator (HRPWM)

5.9.3.1. Clock

Each HRPWMCLK uses PWMCLK from its corresponding PWM module.

Figure 49 HRPWM Clock



2025-11-26

Table 102 HRPWM Frequency

Symbol	Parameter	Min	Typ	Max	Unit
$f_{(HRPWM)}$	Frequency, SYSCLK	60			MHz

Table 103 High-Resolution PWM Characteristics

Parameter	Min	Typ	Max	Unit
Micro-edge positioning (HRP) step size (1)		150	310	ps

Note: Applications using HRPWM should use the HRP scale factor optimizer (SFO) estimation software function.

(1) HRP step size is greatest at high temperature and minimum VDD. It increases as temperature rises and voltage falls, and decreases as temperature falls and voltage rises.

5.9.4. Quadrature Encoder Pulse (QEP)

5.9.4.1. QEP Electrical Characteristics and Timing

Table 104 QEP Timing Requirements

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(QEPP)}$	QEP input period	Synchronous (2)	$2t_{c(SYSCLK)}$		Period
		With input qualification (1)	$2[1t_{c(SYSCLK)}+ t_{w(IQSW)}]$		
$t_{w(INDEXH)}$	QEP index input high time	Synchronous (2)	$2t_{c(SYSCLK)}$		Period
		With input qualification (1)	$2t_{c(SYSCLK)}+ t_{w(IQSW)}$		
$t_{w(INDEXL)}$	QEP index input low time	Synchronous (2)	$2t_{c(SYSCLK)}$		Period
		With input qualification (1)	$2t_{c(SYSCLK)}+ t_{w(IQSW)}$		
$t_{w(STROBH)}$	QEP strobe high time	Synchronous (2)	$2t_{c(SYSCLK)}$		Period
		With input qualification (1)	$2t_{c(SYSCLK)}+ t_{w(IQSW)}$		
$t_{w(STROBL)}$	QEP strobe input low time	Synchronous (2)	$2t_{c(SYSCLK)}$		Period
		With input qualification (1)	$2t_{c(SYSCLK)}+ t_{w(IQSW)}$		

Note:

(1) See General-Purpose Input Timing Requirements for input qualification parameters.

(2) Do not use GPIO GPxQSELn asynchronous mode for QEP input pins.

Table 105 QEP Switching Characteristics

Symbol	Parameter	Min	Max	Unit
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		$5t_{c(SYSCLK)}$	Period
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position-compare synchronization output		$7t_{c(SYSCLK)}$	Period

5.10. Communication Peripherals

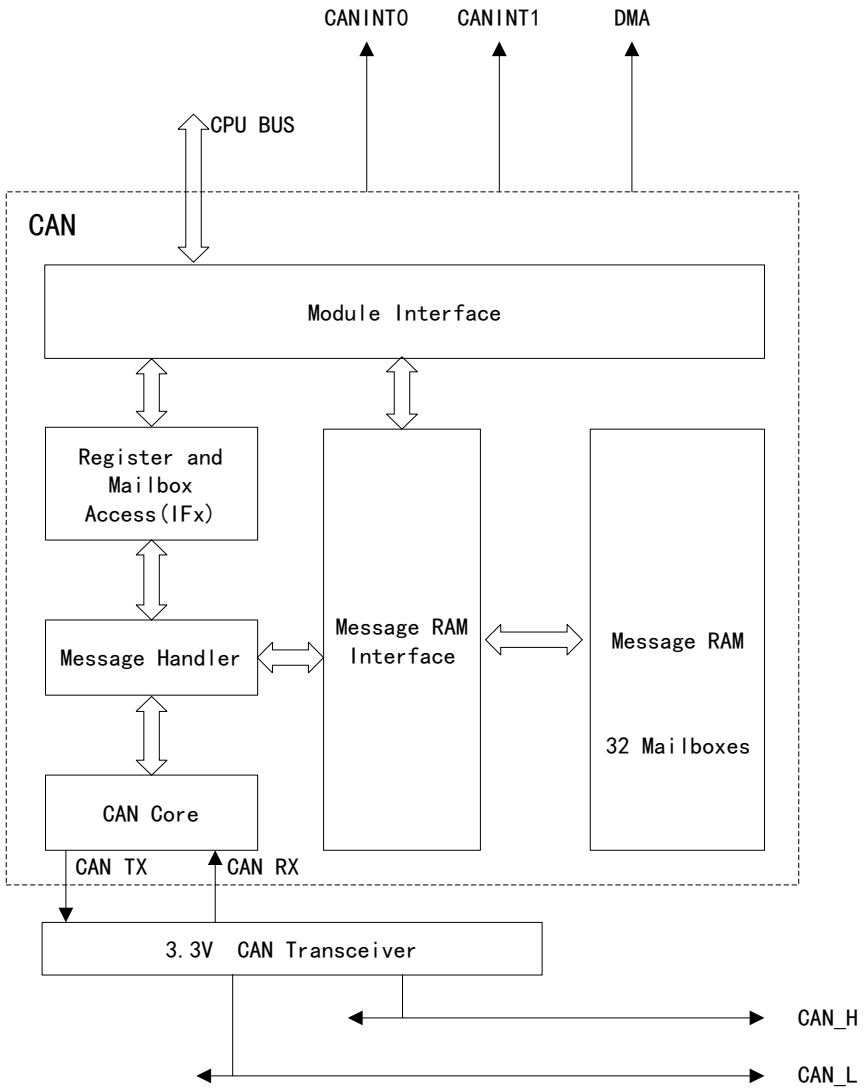
5.10.1. Controller Area Network (CAN)

5.10.1.1. Main Features

(1) Complies with ISO11898-1 (Bosch® CAN Protocol Specification 2.0 A and B)
(2) Bit rates up to 1Mbps
(3) Multiple clock sources
(4) DMA support
(5) 32 message objects (mailboxes), each providing:
- Configurable receive or transmit operation
- Configurable standard (11-bit) or extended (29-bit) identifier
- Programmable identifier acceptance mask
- Data and remote frame support
- Storage for 0 to 8 data bytes
- Parity checking for configuration and data RAM

(6) Individual identifier mask per message object
(7) Programmable FIFO mode for message objects
(8) Programmable loopback mode for self-test
(9) Suspend mode for debug support
(10) Software module reset
(11) Automatic bus-on after bus-off using a programmable 32-bit timer
(12) 2 interrupt lines

Figure 50 Block Diagram



5.10.2. Controller Area Network with Flexible Data Rate (CAN FD)

5.10.2.1. Main Features

(1) Complies with CAN Protocol 2.0A/B and ISO 11898-1:2015
(2) Full CAN FD support (up to 64 data bytes)
(3) AUTOSAR and SAE J1939 support
(4) Flexible message RAM allocation (maximum configurations below apply to devices with 1024 × 32-bit words of message RAM)
- Up to 32 dedicated transmit buffers
- Configurable transmit FIFO with up to 32 elements
- Configurable transmit queue with up to 32 elements
- Configurable transmit event FIFO with up to 32 elements
- Up to 64 dedicated receive buffers
- Two configurable receive FIFOs, each with up to 64 elements
- Up to 128 filter elements

(5) Loopback mode for self-test

(6) Maskable interrupts (two configurable interrupt lines, uncorrectable ECC, and clock stop/wake-up)
(7) Two clock domains (CAN clock/host clock)
(8) Message RAM ECC checking
(9) Clock stop and wake-up support
(10) Internal and external timestamps

Unsupported features:

- Host bus firewall
- Clock calibration
- Debug over CAN

5.10.3. Inter-Integrated Circuit (I2C)

5.10.3.1. I2C Electrical Data and Timing

Table 106 I2C Timing Requirements

No.	Symbol	Parameter	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
T0	f_{mod}	I2C module frequency	7	12	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	START hold time, SDA falling to SCL falling delay	4.0		0.6		μs
T2	$t_{su(SCL-SDA)START}$	Repeated START setup time, SCL rising to SDA falling delay	4.0		0.6		μs
T3	$t_{h(SCL-DAT)}$	Data hold time after SCL falling	0		0		μs
T4	$t_{su(DAT-SCL)}$	Data setup time before SCL rising	250		100		ns
T5	$t_{r(SDA)}$	Rise time, SDA		1000	20	300	ns
T6	$t_{r(SCL)}$	Rise time, SCL		1000	2	300	ns
T7	$t_{f(SDA)}$	Fall time, SDA		300	11.4	300	ns
T8	$t_{f(SCL)}$	Fall time, SCL		300	11.4	300	ns
T9	$t_{su(SCL-SDA)STOP}$	STOP setup time, SCL rising to SDA rising delay	4.0		0.6		μs
T10	$t_{w(SP)}$	Spike pulse duration suppressed by filter	0	50	0	50	ns
T11	Cb	Capacitive load per bus		400		400	pF

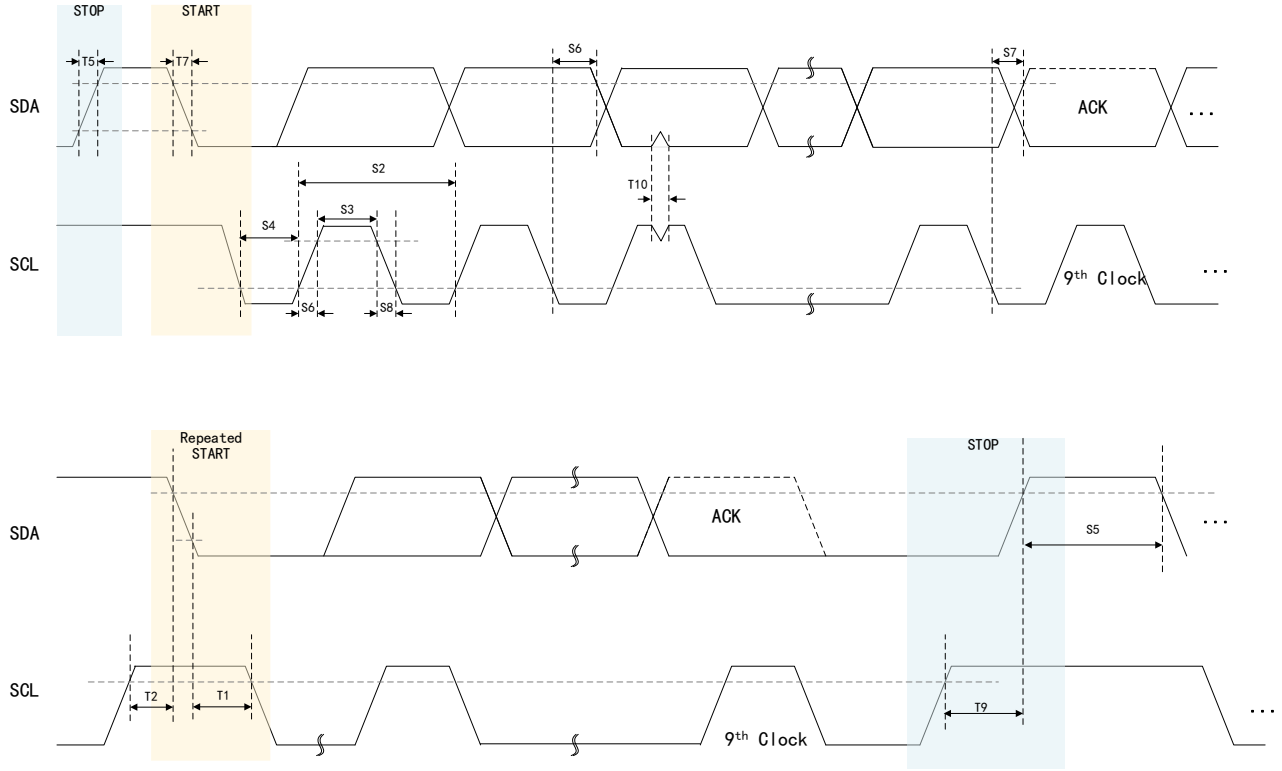
Table 107 I2C Switching Characteristics

No.	Symbol	Parameter	Test conditions	Standard mode		Fast mode		Unit
				Min	Max	Min	Max	
S1	f_{SCL}	SCL clock frequency		0	100	0	400	kHz
S2	T_{SCL}	SCL clock period		10		2.5		μs

S3	$t_{w(SCLL)}$	Pulse duration, SCL low		4.7		1.3		μs
S4	$t_{w(SCLH)}$	Pulse duration, SCL high		4.0		0.6		μs
S5	t_{BUF}	Bus free time between STOP and START		4.7		1.3		μs
S6	$t_{v(SCL-DAT)}$	Data valid time after SCL falling			3.45	0.9		μs
S7	$t_{v(SCL-ACK)}$	Acknowledgment valid time after SCL falling			3.45	0.9		μs
S8	I_I	Input current on pins	0.1 V_{bus} < V_i< 0.9 V_{bus}	-10	10	-10	10	μA

Configure I2C module clock Fmod between 7MHz and 12MHz to meet all I2C protocol timing specifications.

Figure 51 I2C Timing Diagram



5.10.4. Power Management Bus (PMBUS) Interface

5.10.4.1. PMBUS Electrical Data and Timing

Table 108 PMBUS Electrical Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IL}	Valid low-level input voltage				0.8	V
V_{IH}	Valid high-level input voltage		2.1		VDDIO	V
V_{OL}	Low-level output voltage	At Ipullup = 4mA			0.4	V

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{OL}	Low-level output current	VOL ≤ 0.4V	4			mA
t_{SP}	Spike pulse width suppressed by input filter		0		50	ns
I_i	Input leakage current per pin	0.1Vbus < Vi < 0.9Vbus	-10		10	μA
C_i	Capacitance per pin				10	pF

Table 109 PMBUS Switching Characteristics

Symbol	Parameter	Test conditions	Standard mode			Fast mode			Unit
			Min	Typ	Max	Min	Typ	Max	
f_{SCL}	SCL clock frequency		10		100	10		400	kHz
t_{BUF}	Bus free time between STOP and START		4.7			1.3			μs
$t_{HD;STA}$	START hold time - SDA falling to SCL falling delay		4			0.6			μs
$t_{SU;STA}$	Repeated START setup time - SCL rising to SDA falling delay		4.7			0.6			μs
$t_{SU;STO}$	STOP setup time - SCL rising to SDA rising delay		4			0.6			μs
$t_{HD;DAT}$	Data hold time after SCL falling		300			300			ns
$t_{SU;DAT}$	Data setup time before SCL rising		250			100			ns
$t_{Timeout}$	Clock low timeout		25		35	25		35	ms
t_{LOW}	SCL low period		4.7			1.3			μs
t_{HIGH}	SCL high period		4		50	0.6		50	μs
$t_{LOW;SEXT}$	Cumulative clock low extension (slave)	From START to STOP			25			25	ms
$t_{LOW;MEXT}$	Cumulative clock low extension (master)	Within each byte			10			10	ms
t_r	SDA and SCL rise time	5% to 95%			1000	20		300	ns
t_f	SDA and SCL fall time	95% to 5%			300	20		300	ns

5.10.5. Serial Communication Interface (UART)

Digital communication uses standard non-return-to-zero (NRZ) format. Both UART transmitter and receiver have a 16-level FIFO and independent enable and interrupt bits. They operate independently in half duplex or simultaneously in full duplex. A 16-bit baud selection register programs the bit rate.

5.10.6. Serial Peripheral Interface (SPI)

5.10.6.1. Non-High-Speed Master Mode Timing

Table 110 SPI Non-High-Speed Master Mode Switching Characteristics

No.	Symbol	Parameter	(BRR+1)	Clock phase = 0		Clock phase = 1		Unit
				Min	Max	Min	Max	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	$0.5t_{c(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 3$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M} + 3$	$0.5t_{c(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 3$	
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid	Even		5	$0.5t_{c(SPC)M} - 4$		ns
			Odd		5	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$		
5	$t_{v(SIMO)M}$	Valid time, SPISIMO after SPICLK	Even	$0.5t_{c(SPC)M} - 6$		$0.5t_{c(SPC)M} - 6$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		
23	$t_{d(SPC)M}$	Delay time, SPISTEn active to SPICLK	Even, odd	$1.5t_{c(SPC)M} - 3t_{c(APBCLK)} - 3$		$2t_{c(SPC)M} - 3t_{c(APBCLK)} - 3$		ns
24	$t_{d(STE)M}$	Delay time, SPICLK to SPISTEn	Even	$0.5t_{c(SPC)M} - 6$		$0.5t_{c(SPC)M} - 6$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)}$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		

		inactive		) – 3				

Table 111 SPI Non-High-Speed Master Mode Timing Requirements

No.	Symbol	Parameter	(BRR + 1) condition	Min	Max	Unit
8	$t_{su(SOMI)M}$	Setup time, SPISOMI valid before SPICLK	Even, odd	20		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	Even, odd	0		ns

Figure 52 Non-High-Speed SPI Master External Timing (Clock Phase = 0)

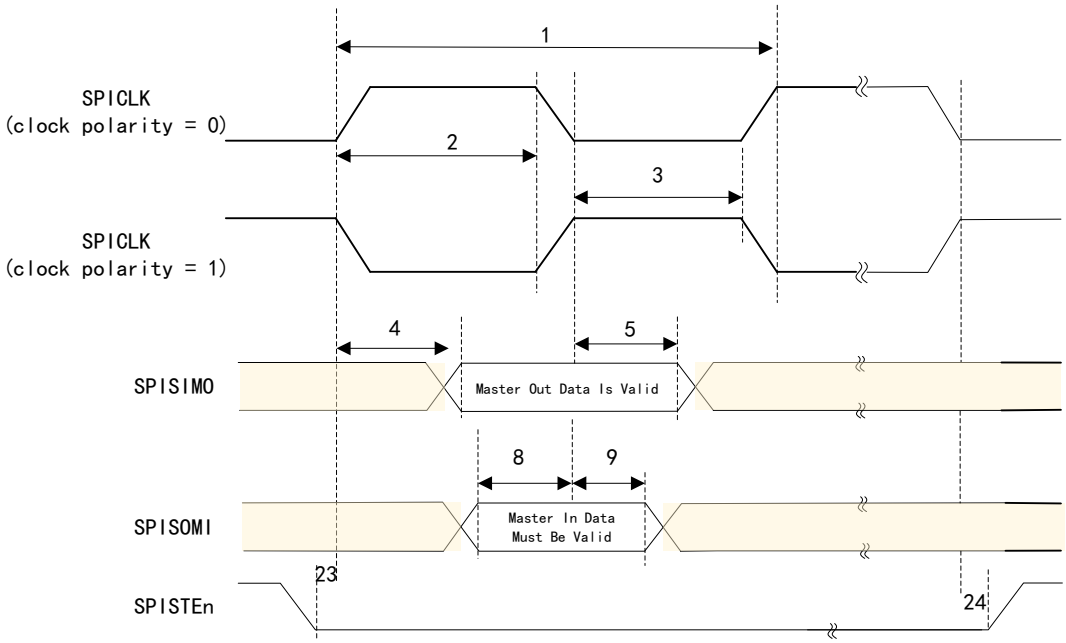
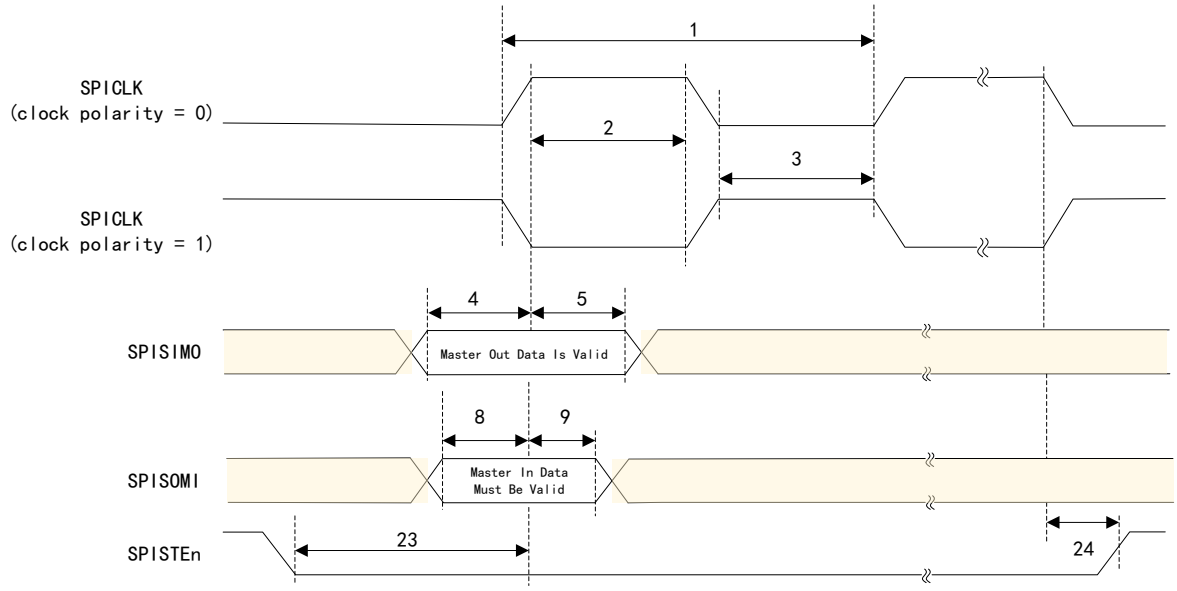


Figure 53 Non-High-Speed SPI Master External Timing (Clock Phase = 1)



5.10.6.2. Non-High-Speed Slave Mode Timing

Table 112 SPI Non-High-Speed Slave Mode Switching Characteristics

No.	Symbol	Parameter	Min	Max	Unit
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		16	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI after SPICLK	0		ns

Table 113 SPI Non-High-Speed Slave Mode Timing Requirements

No.	Symbol	Parameter	Min	Max	Unit
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK, first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, second pulse	$2t_{c(SYSCLK)} - 1$		ns
19	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(SIMO)S}$	Hold time, SPISIMO valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, SPISTE active before SPICLK (clock phase = 0)	$2t_{c(SYSCLK)} + 2$		ns
		Setup time, SPISTE active before SPICLK (clock phase = 1)	$2t_{c(SYSCLK)} + 22$		ns
26	$t_{h(STE)S}$	Hold time, SPISTE inactive after SPICLK	$1.5t_{c(SYSCLK)}$		ns

Figure 54 Non-High-Speed SPI Slave External Timing (Clock Phase = 0)

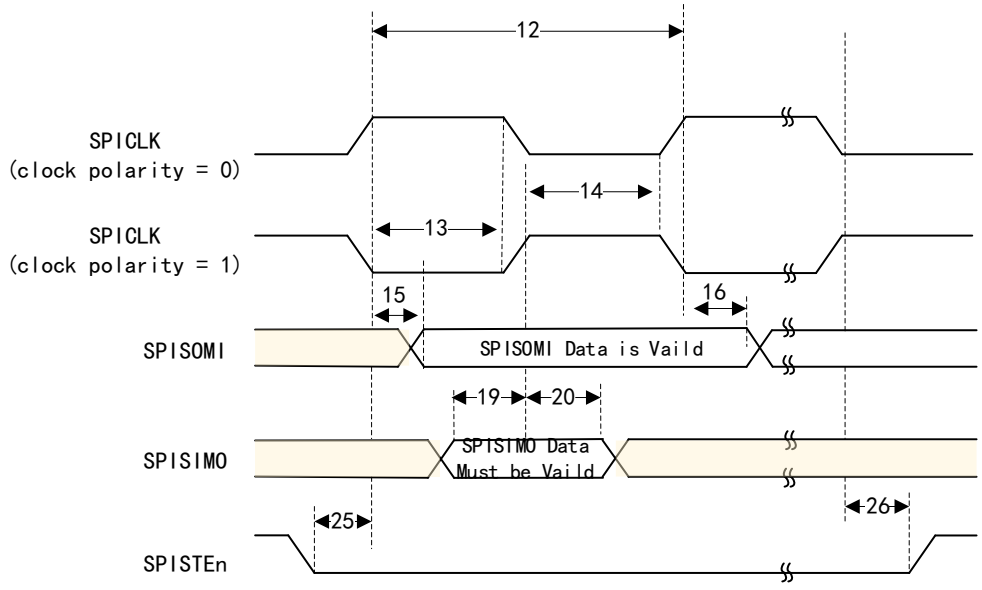
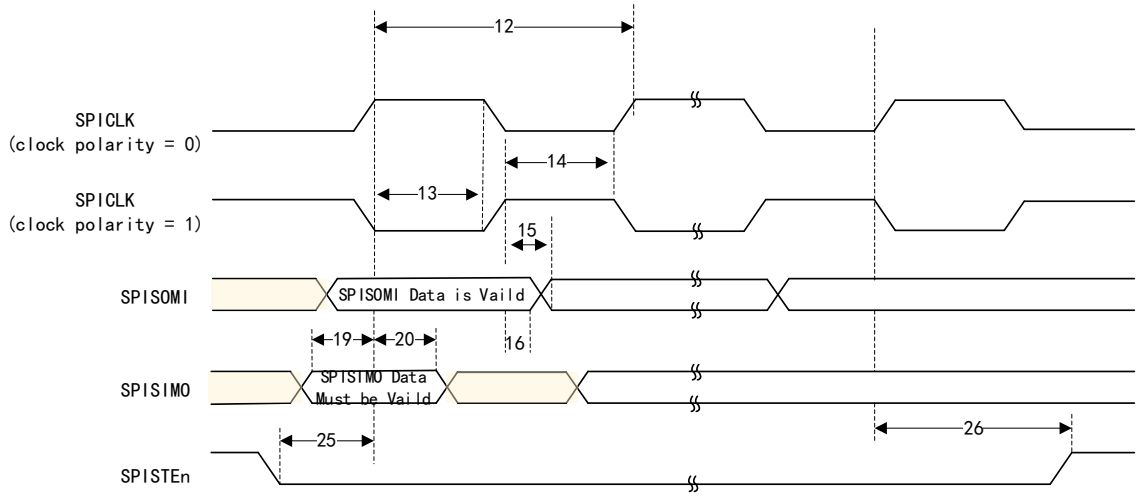


Figure 55 Non-High-Speed SPI Slave External Timing (Clock Phase = 1)



5.10.6.3. High-Speed Master Mode Timing

Table 114 SPI High-Speed Master Mode Switching Characteristics

No.	Symbol	Parameter	BRR+1	Clock phase = 0		Clock phase = 1		Unit
				Min	Max	Min	Max	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M}$ - 1	$0.5t_{c(SPC)M}$ + 1	$0.5t_{c(SPC)M}$ - 3	$0.5t_{c(SPC)M}$ + 3	ns
			Odd	$0.5t_{c(SPC)M}$ +	$0.5t_{c(SPC)M}$ +$0.5t_{c(LSPCLK}$	$0.5t_{c(SPC)M}$ - $0.5t_{c(LSPCLK)}$	$0.5t_{c(SPC)M}$ - $0.5t_{c(LSPCLK}$	

				$0.5t_{c(LSPCLK)}$ – 1	) +1	– 3	) + 3	
3	$t_{w\ (SPC2)\ M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)\ M}$ – 1	$0.5t_{c(SPC)\ M}$ +1	$0.5t_{c(SPC)\ M-3}$	$0.5t_{c(SPC)\ M}$ + 3	ns
			Odd	$0.5t_{c(SPC)\ M}$ – $0.5t_{c(\ LSPCLK\ )}$ – 1	$0.5t_{c(SPC)\ M}$ – $0.5t_{c(\ LSPCLK)}$ +1	$0.5t_{c(SPC)\ M}$ +$0.5t_{c(LSPCLK\ )}$ – 3	$0.5t_{c(SPC)\ M}$ + $0.5t_{c(\ LSPCLK\ )}$ + 3	
4	$t_{d\ (SIMO)\ M}$	Delay time, SPICLK to SPISIMO valid	Even		3	$0.5t_{c(SPC)\ M}$ - 4		ns
			Odd		3	$0.5t_{c(SPC)\ M}$ +$0.5t_{c(LSPCLK\ )}$ – 1		
5	$t_{v\ (SIMO)\ M}$	Valid time, SPISIMO after SPICLK	Even	$0.5t_{c(SPC)\ M}$ - 4		$0.5t_{c(SPC)\ M}$ - 6		ns
			Odd	$0.5t_{c(SPC)\ M}$ - $0.5t_{c(\ LSPCLK\ )}$ – 1		$0.5t_{c(SPC)\ M}$ - $0.5t_{c(\ LSPCLK)}$ – 1		
23	$t_{d(SPC)\ M}$	Delay time, SPISTEn active to SPICLK	Even, odd	$1.5t_{c(SPC)\ M}$ -$3t_{c\ (APBCLK)}$ –1		$2t_{c(SPC)}$ M - $3t_{c\ (APBCLK)}$ – 1		ns
24	td(STE) M	Delay time, SPICLK to SPISTEn inactive	Even	$0.5t_{c(SPC)\ M}$ - 4		$0.5t_{c(SPC)\ M}$ - 6		ns
			Odd	$0.5t_{c(SPC)\ M}$ - $0.5t_{c(\ LSPCLK\ )}$ – 1		$0.5t_{c(SPC)\ M}$ - $0.5t_{c(\ LSPCLK)}$ – 1		

Table 115 SPI High-Speed Master Mode Timing Requirements

No.	Symbol	Parameter	(BRR + 1) condition	Min	Max	Unit
8	$t_{su(SOMI)\ M}$	Setup time, SPISOMI valid before SPICLK	Even, odd	2		ns
9	$t_{h(SOMI)\ M}$	Hold time, SPISOMI valid after SPICLK	Even, odd	11		ns

Figure 56 High-Speed SPI Master External Timing (Clock Phase = 0)

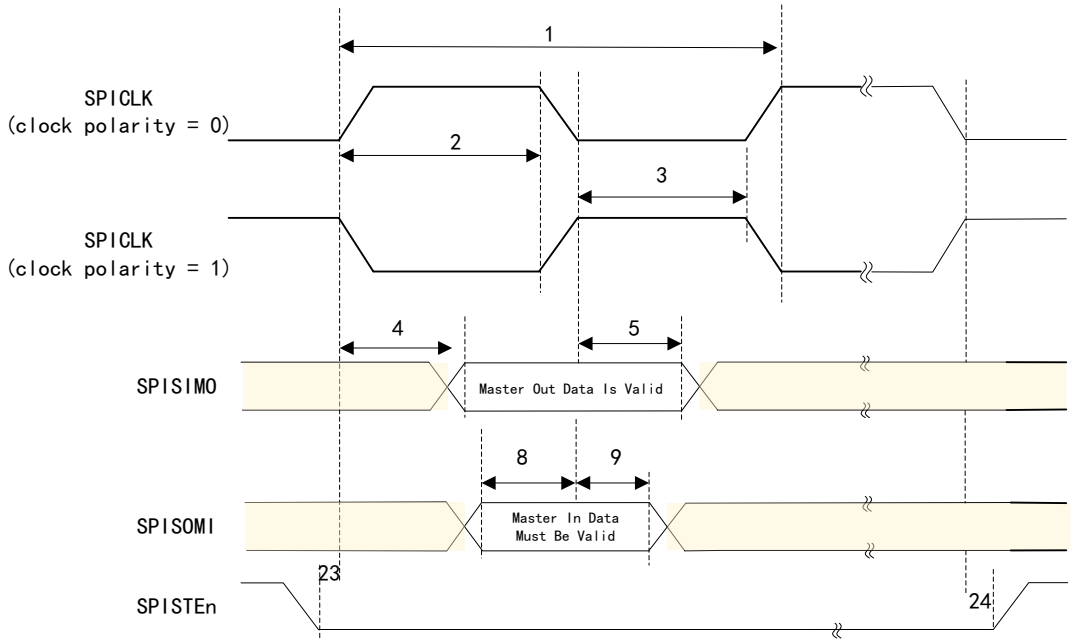
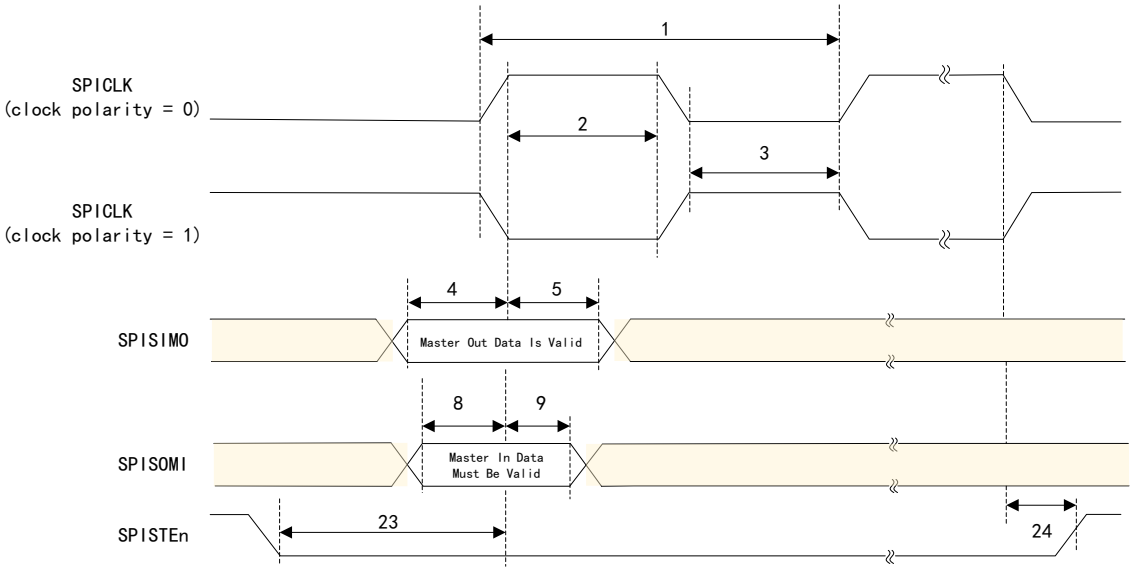


Figure 57 High-Speed SPI Master External Timing (Clock Phase = 1)



5.10.6.4. High-Speed Slave Mode Timing

Table 116 SPI High-Speed Slave Mode Switching Characteristics

No.	Symbol	Parameter	Min	Max	Unit
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		14	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI after SPICLK	0		ns

Table 117 SPI High-Speed Slave Mode Timing Requirements

No.	Symbol	Parameter	Min	Max	Unit
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(APBCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK, first pulse	$2t_{c(APBCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, second pulse	$2t_{c(APBCLK)} - 1$		ns

No.	Symbol	Parameter	Min	Max	Unit
19	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(APBCLK)}$		ns
20	$t_{h(SIMO)S}$	Hold time, SPISIMO valid after SPICLK	$1.5t_{c(APBCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, SPISTE active before SPICLK	$1.5t_{c(APBCLK)}$		ns
26	$t_{h(STE)S}$	Hold time, SPISTE inactive after SPICLK	$1.5t_{c(APBCLK)}$		ns

Figure 58 High-Speed SPI Slave External Timing (Clock Phase = 0)

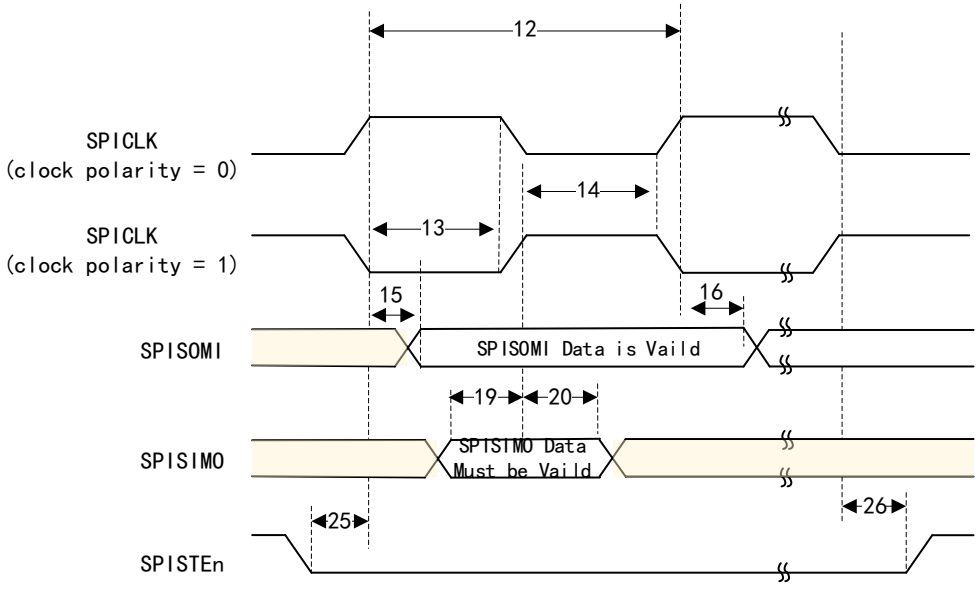
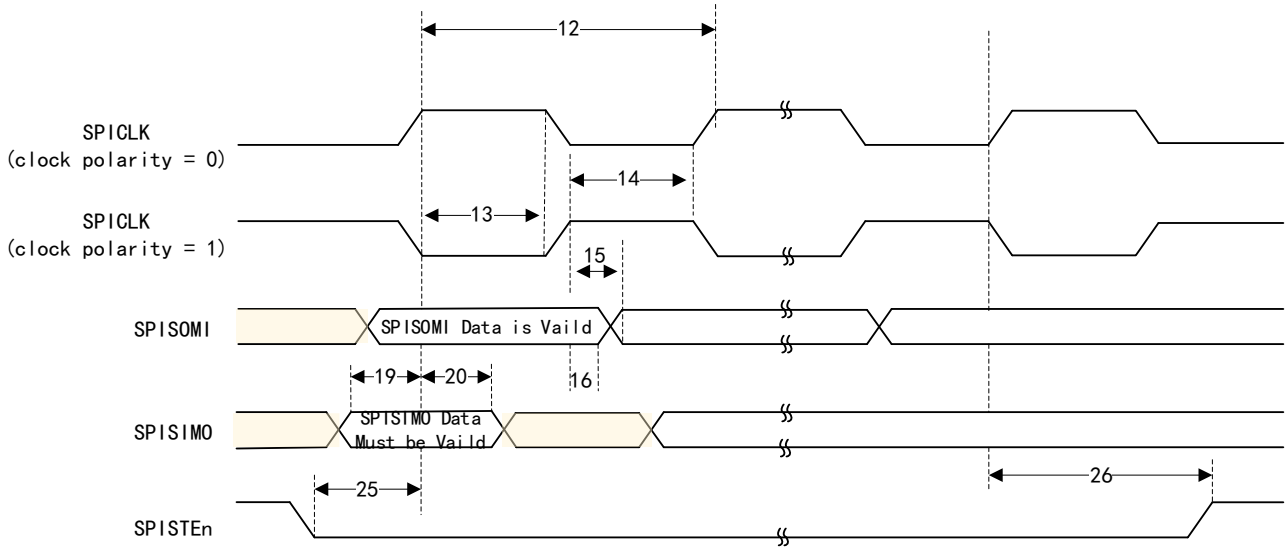


Figure 59 High-Speed SPI Slave External Timing (Clock Phase = 1)



5.10.7. Local Interconnect Network (LIN)

LIN complies with LIN 2.1 as defined in LIN Specification Package Revision 2.1. This low-cost serial interface serves applications where CAN is too costly, such as

small automotive subnetworks for interior lighting or window control. LIN uses UART serial data formatting. A single master and multiple slaves use message identifiers for multicast transmission among network nodes. The module can operate as UART or LIN.

5.11. Dual-Clock Comparator (DCCOMP)

5.11.1. Introduction

DCCOMP evaluates and monitors an input clock against a more accurate and reliable clock. It detects faults in clock sources or clock structures to enhance system safety.

5.11.2. Main Features

(1) Single-sequence mode for spot measurements
(2) Selectable clock source for each counter
(3) Continuous monitoring without application intervention
(4) Programmable tolerance window defined in reference clock cycles
(5) Allows the application to ensure a fixed frequency ratio between two clocks

5.11.3. Block Diagram

Figure 60 DCCOMP System Connections

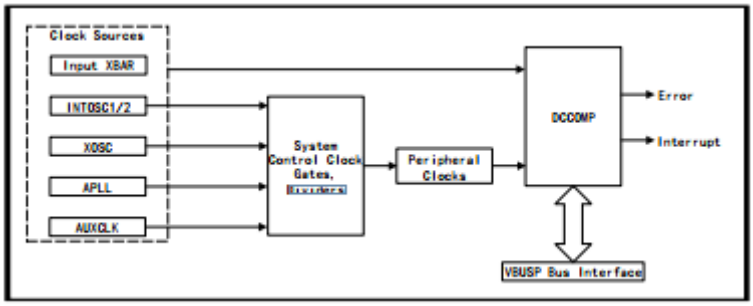
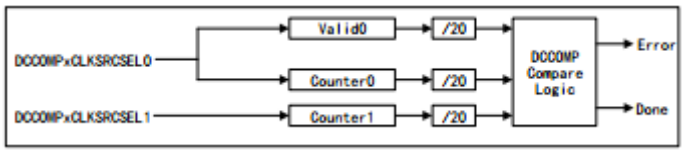


Figure 61 DCCOMP Block Diagram



5.11.4. Functional Description

As shown in the block diagram, DCCOMP contains Counter0, Counter1, and Valid0. Users first define their preload values. When DCCOMP is enabled, Counter0 and Counter1 count down at Clock0 and Clock1 rates, respectively. When Counter0 reaches 0, Valid0 counts down at the Clock0 rate. If Counter1 reaches 0 within this valid window, no error occurs and Clock1 is within the configured tolerance.

5.11.4.1. DCCOMP Counters

Configure Counter0 and Counter1 according to the Clock0-to-Clock1 ratio: FCLK0*Counter1 = FCLK1*Counter0. Valid0 provides tolerance and is configured based on DCCOMP error.

Error Sources in Counter Configuration

Clock0 and Clock1 are asynchronous, so counter starts and stops are not synchronized. Consider the following error sources when configuring counters:

(1) Digitization error equals 8 Clock0 cycles.

(2) DCCOMP error due to asynchronous Clock0 and Clock1 (frequency-dependent)

- If FCLK1 is unknown, asynchronous error = 2*[max(FSYSCLK/FCLK0)] + 2, in Clock0 cycles.
- If FCLK1 > FCLK0, asynchronous error = 2*(FSYSCLK/FCLK0) + 2, in Clock0 cycles.
- If FCLK1 < FCLK0, asynchronous error = 2*(FCLK0/FCLK1) + 2*[max(FSYSCLK/FCLK0)], in Clock0 cycles.

Calculating Total DCCOMP Error

DCCOMP Error Formula

- DCCOMP error = asynchronous error + digitization error, in Clock0 cycles.

DCCOMP error is the measurement error introduced by DCCOMP itself, not the frequency error of the measured clock. Account for it in counter configuration and select an appropriate tolerance, as DCCOMP error determines the measurement window.

Window Formula

- Window = DCCOMP error/(tolerance*0.01), in Clock0 cycles.

For a DCCOMP error of 10 and required tolerance of ±0.1%, the window is 10000 Clock0 cycles.

A tighter tolerance requires larger counter values and a longer measurement window. For example, counter values at 0.1% tolerance exceed those at 0.2%. The application tolerance therefore determines the window in Clock0 cycles.

Allowed Frequency Error Formula

The measured clock may have an expected frequency error, which must also be considered in counter configuration. For example, when an external crystal measures INTOSC1/2, include the allowed INTOSC1/2 frequency tolerance. The formula is:

- Allowed frequency error = (frequency tolerance/100)*window, where error is in Clock0 cycles and tolerance in %.

Total Error Formula

- Total error = DCCOMP error + allowed frequency error

Configuring Counter Values

- CNTSEED0 = window - total error
- CNTSEED1 = (FCLK1/FCLK0)*window
- VALSEED0 = total error*2

The 20-bit Counter1 cannot exceed 1048575. If it would, increase the target tolerance to reduce the measurement window. Minimum tolerance is calculated as:

- Tolerance = [(FCLK1/FCLK0)*DCCOMP error*100]/1048575

5.11.4.2. Single-Shot Test Mode

Enable single-shot mode to perform one countdown. In this mode, DCCOMP stops after Counter0 and Valid0 reach 0.

DCCOMP is automatically disabled at the end of the countdown to prevent further counting. This mode is typically used for spot frequency checks.

Use Case: Verifying PLLRAWCLK Frequency

This example verifies PLL output frequency using XTAL as the reference.

Assumptions:

- XTAL = 10MHz
- PLL output frequency = 100MHz
- SYSCLK = 100MHz
- Allowed frequency tolerance = 0.1%
- DCCOMP tolerance = 0.1%

Measurement sequence:

(1) Set Clock0 for Counter0 and Valid0 to XTAL, and Clock1 for Counter1 to the PLL output clock.
(2) Using the formulas in Calculating DCCOMP Counters, calculate the seeds: CNTSEED0 = 29940, CNTSEED1 = 300000, VALSEED0 = 120.
(3) When DCCOMP is enabled, Counter0/1 count down from their seeds.
(4) When Counter0 reaches 0, it automatically triggers Valid0.
(5) If Valid0 reaches 0 while Counter1 is nonzero, ERRFLG is set and a DCCOMP error is sent to NVIC. Counter1 stops (freezes). Users can enable an interrupt so NVIC generates an interrupt whenever this error occurs.
(6) Before another spot measurement, the application must clear ERRFLG and restart the module.
(7) If no error occurs at sequence completion, SIGMDONEFLG is set and an interrupt is generated. Clear SIGMDONEFLG before restarting DCCOMP.

Error Status

An error occurs in either of these cases:

- Counter1 reaches 0 before Counter0. Clock1 is faster than expected, or Clock0 is slower than expected.
- Counter1 remains nonzero after both Counter0 and Valid0 reach 0. Clock1 is slower than expected.

Any error freezes the counters. The application can then read their values to help determine the cause.

5.11.4.3. Interrupts

DCCOMP generates an interrupt on either event:

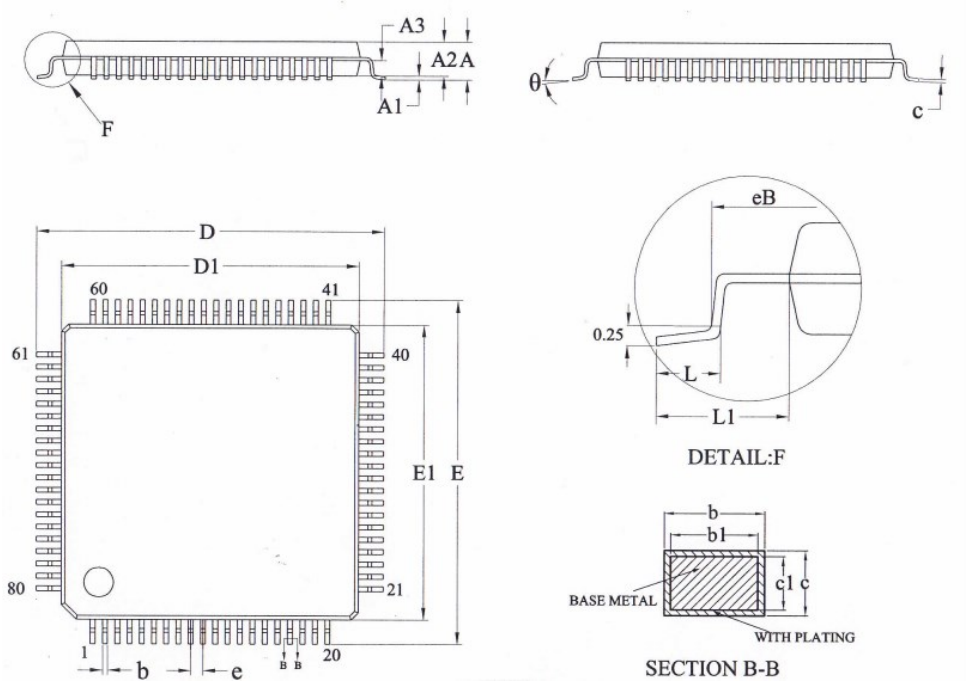
- When DONEEN = 1, an interrupt is generated when counting completes and all counters expire within the specified window (operation complete event).
- When ERREN = 1, an interrupt is generated when a counter fails to expire within the specified window, causing a DCCOMP counting error (error event).

Interrupts from completion and error events are ORed into the DCCOMP interrupt. The ISR must check status flags in DCCOMP_FLG to identify the event.

6. Package Information

6.1. LQFP80 (12mm*12mm) Package Information

Figure 62 LQFP80 Package Drawing



(1) Drawing is not to scale.

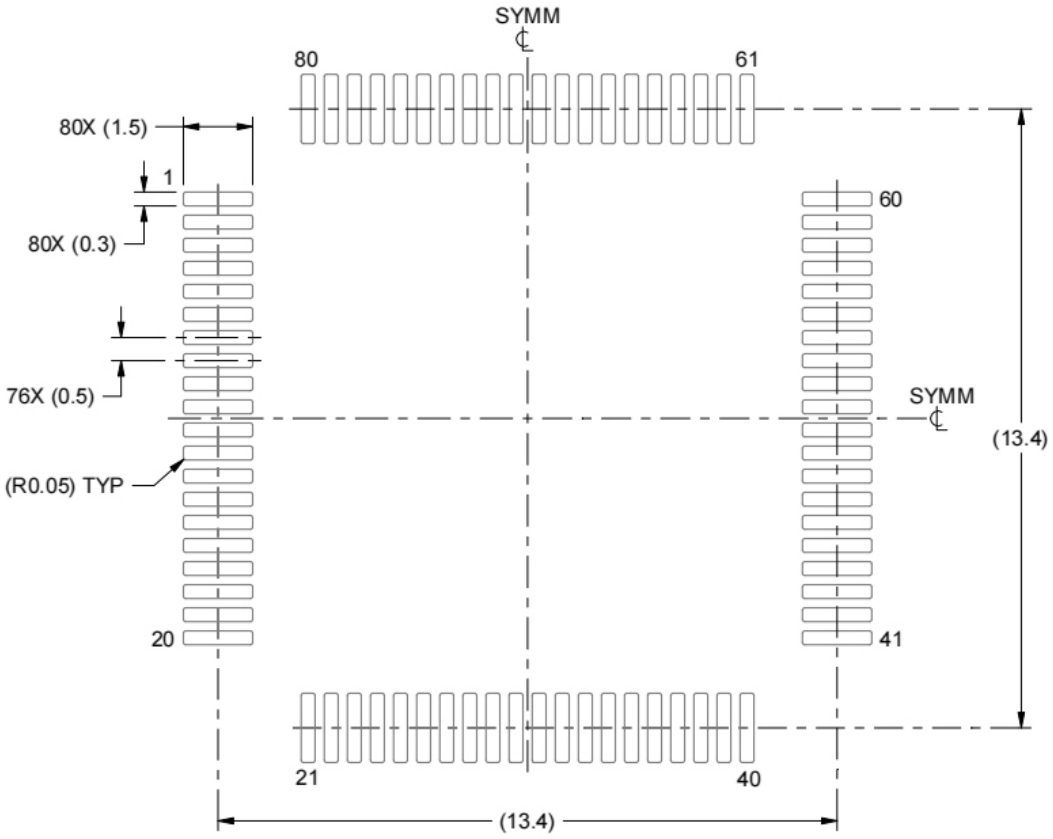
(2) Solder all pins to the PCB.

Table 118 LQFP80 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
eB	13.05	—	13.25
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	7°

Note: Dimensions are in millimeters.

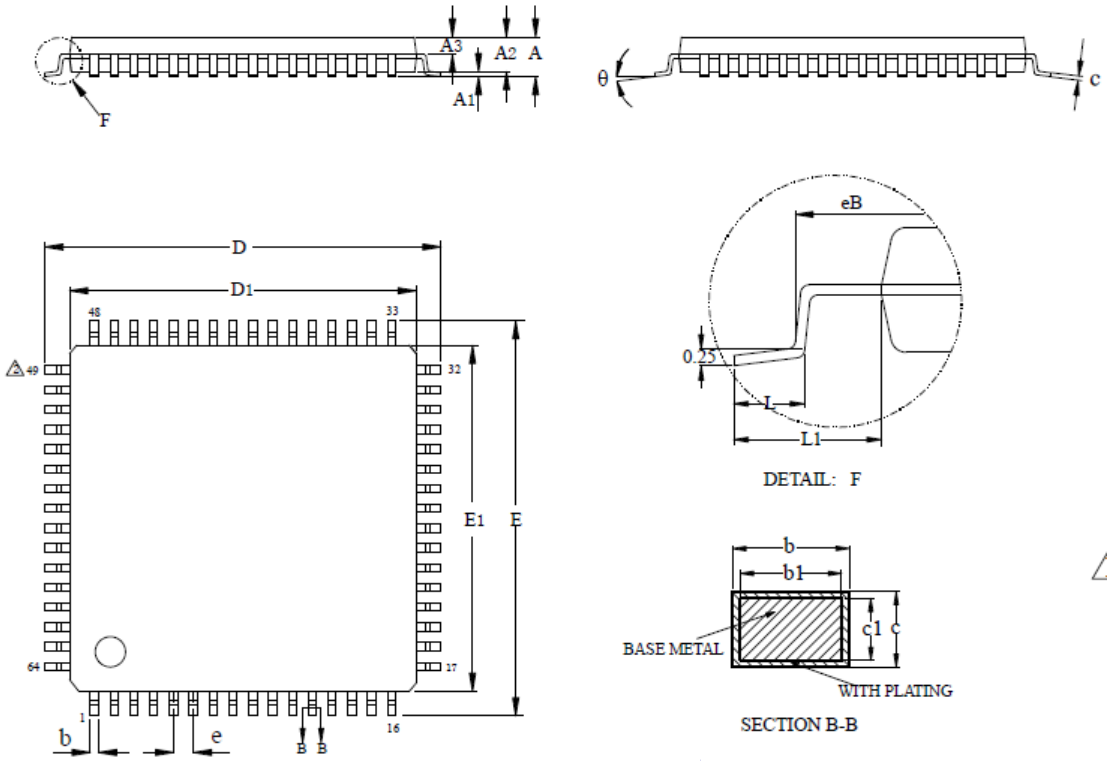
Figure 63 Recommended LQFP80 12x12mm Soldering Layout



Note: Dimensions are in millimeters.

6.2. LQFP64 (10mm*10mm) Package Information

Figure 64 LQFP64 Package Drawing



(1) Drawing is not to scale.

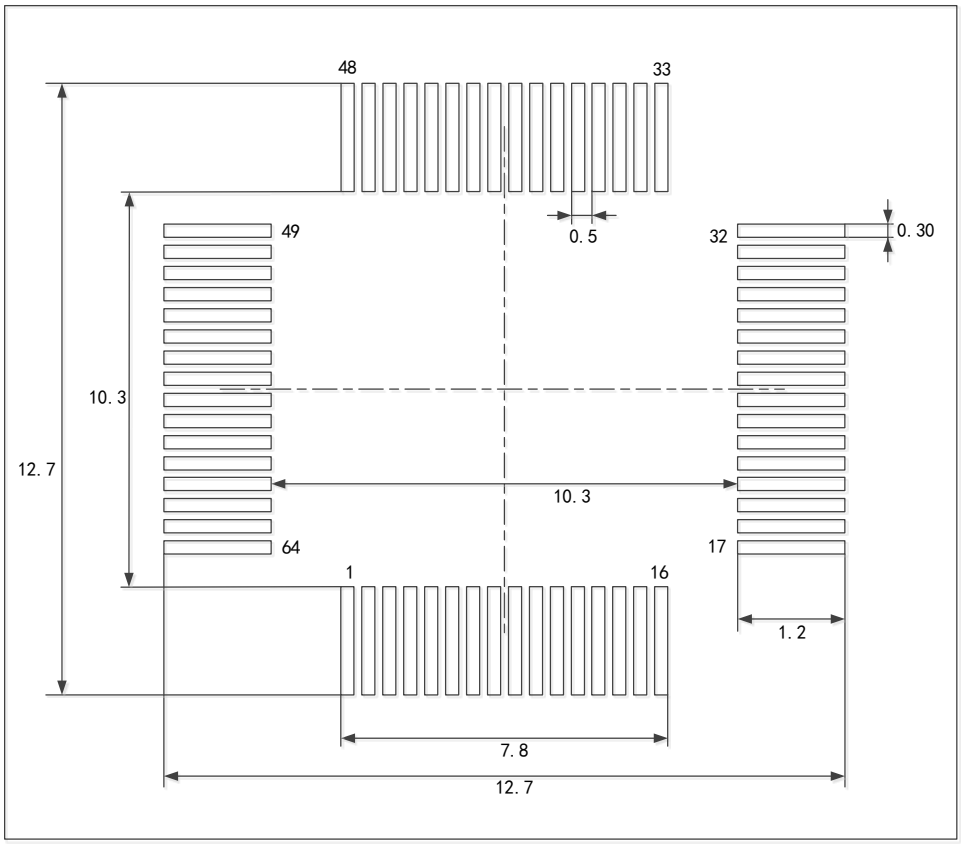
(2) Solder all pins to the PCB.

Table 119 LQFP64 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
eB	11.05	—	11.25
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Note: Dimensions are in millimeters.

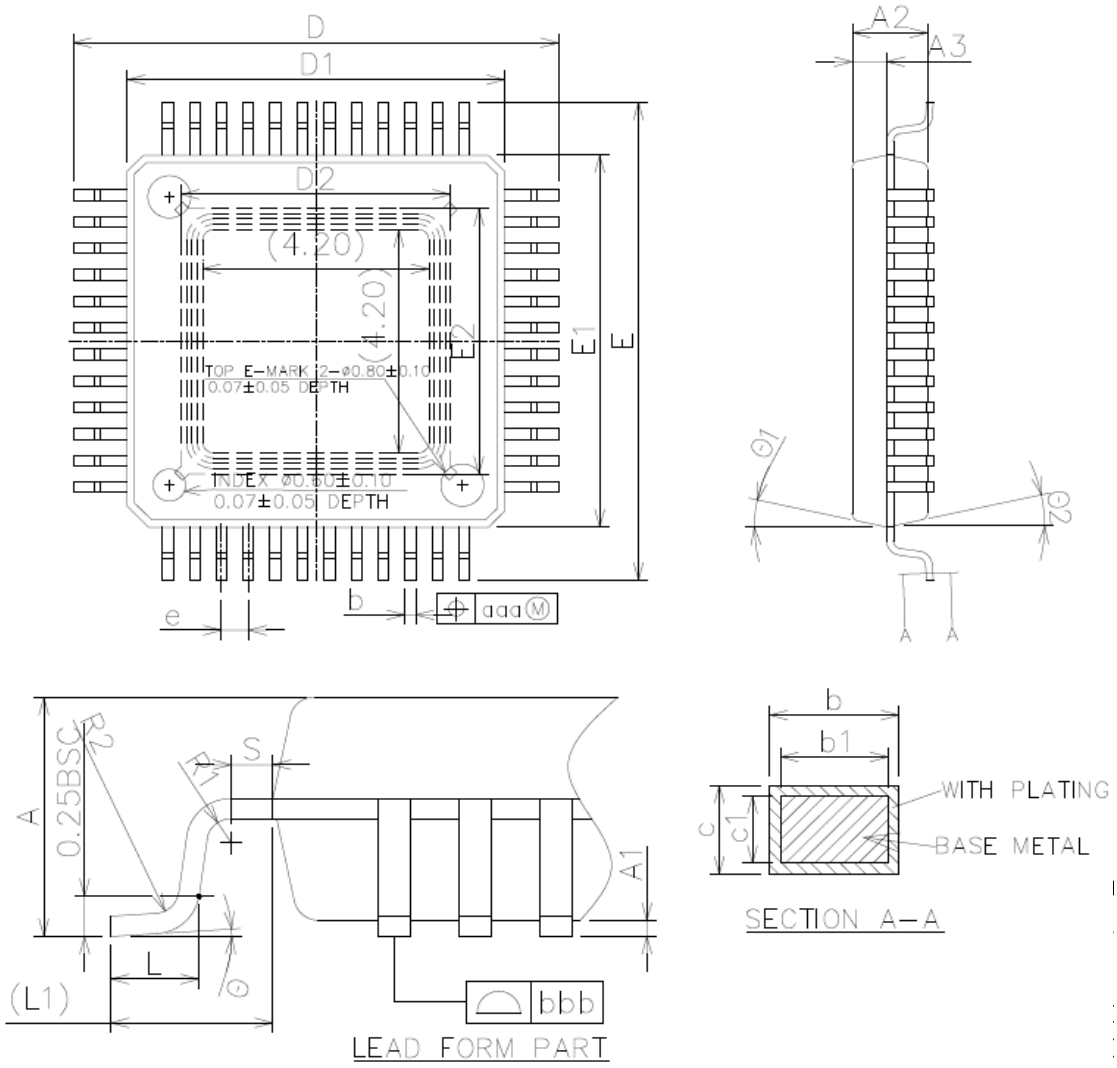
Figure 65 Recommended LQFP64 10x10mm Soldering Layout



Note: Dimensions are in millimeters.

6.3. HTQFP48 (7mm*7mm) Package Information

Figure 66 HTQFP48 Package Drawing



(1) Drawing is not to scale.

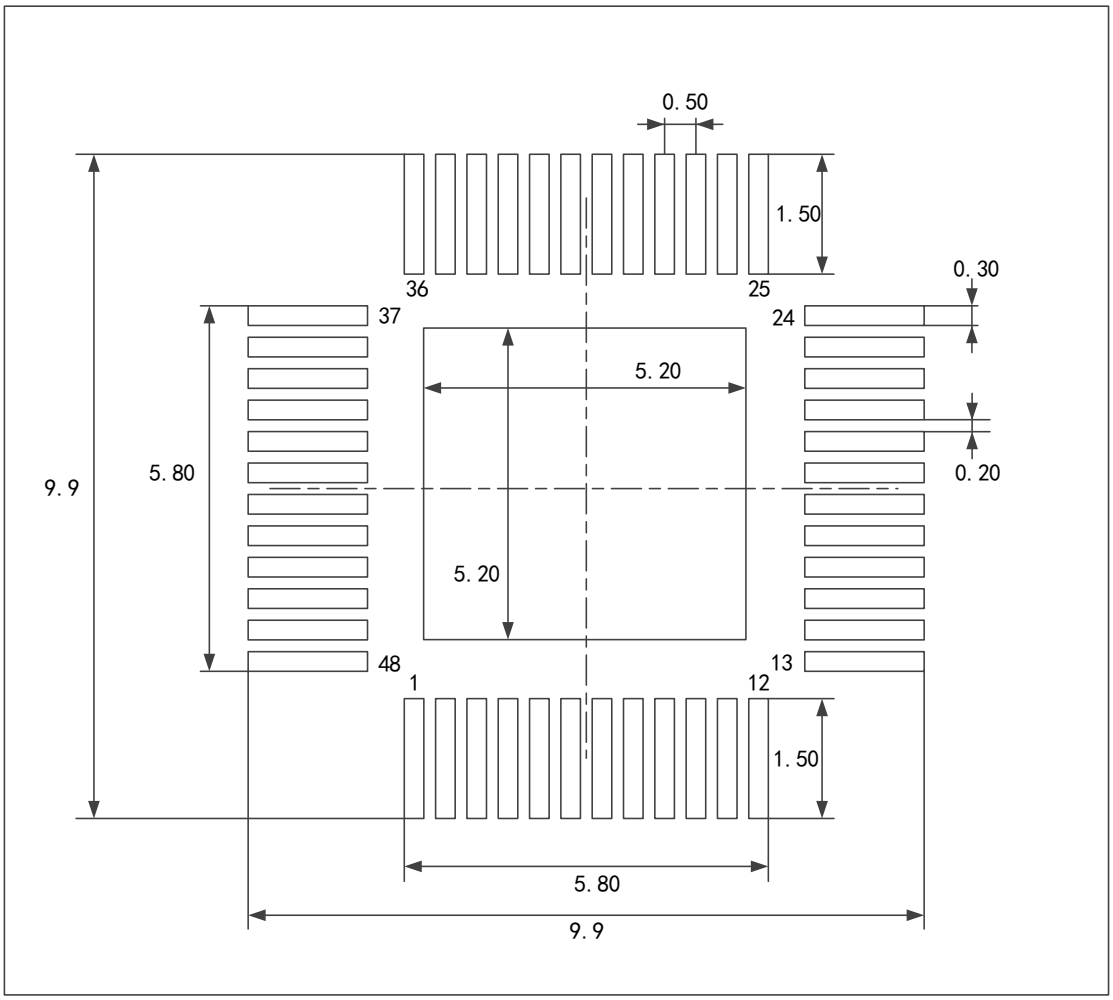
(2) Solder all pins to the PCB.

Table 120 HTQFP48 Package Data

SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
A3	0.39	0.44	0.49
b	0.17	—	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	0.127	0.16
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
D2	5.000 REF		
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
E2	5.000 REF		
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°
aaa	0.08		
bbb	0.08		

Note: Dimensions are in millimeters.

Figure 67 Recommended HTQFP48 7x7mm Soldering Layout



Note: Dimensions are in millimeters.

6.4. VQFN32 (5mm*5mm) Package Information

Figure 68 VQFN32 Package Drawing

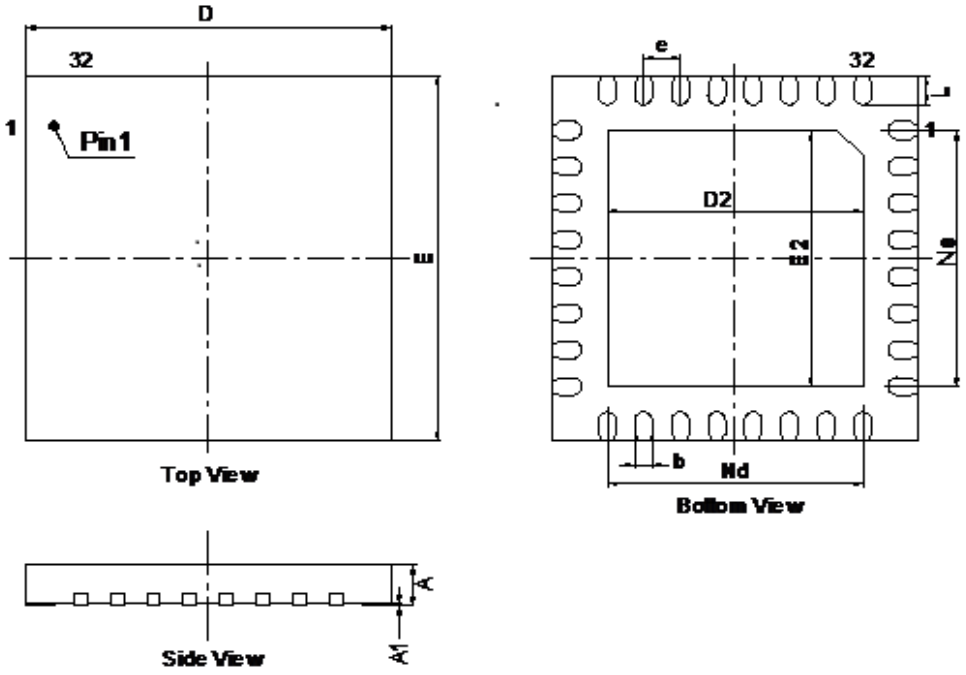
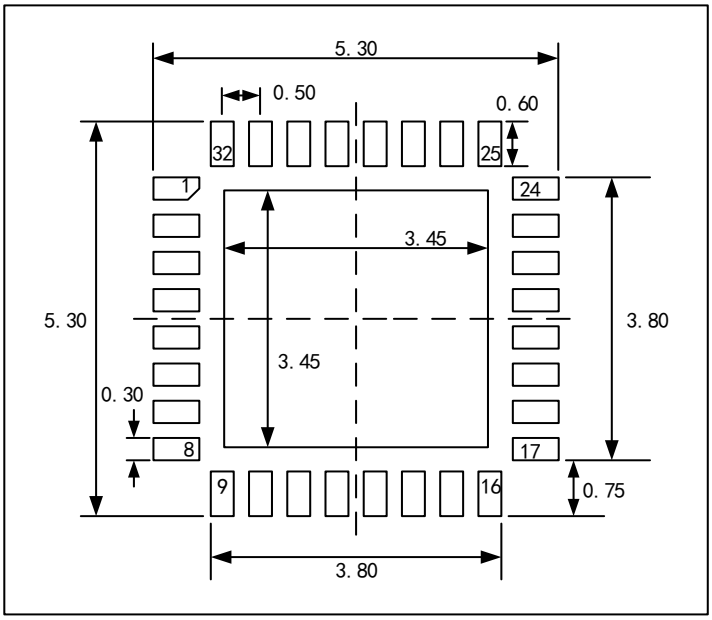


Table 121 VQFN32 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.5	0.55	0.6
A1	0	0.02	0.05
b	0.19	0.24	0.29
D	4.9	5	5.1
D2	3.4	3.5	3.6
e	0.50BSC		
Nd	3.50BSC		
E	4.9	5	5.1
E2	3.4	3.5	3.6
Ne	3.50BSC		
L	0.35	0.4	0.45

Figure 69 Recommended VQFN32 Soldering Layout



6.5. Package Marking

Figure 70 LQFP and VQFN Package Marking

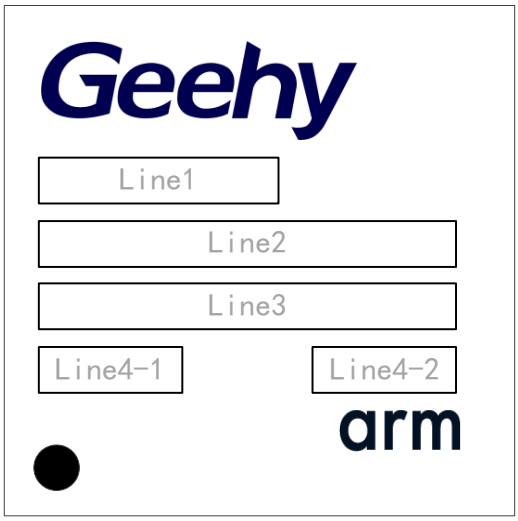


Table 122 LQFP and VQFN Marking Description

Symbols and logos	Description
Geehy	Geehy
Line1	Product series
Line2	Product model
Line3	Product lot number
Line4-1	Internal traceability code
Line4-2	Year and week

Symbols and logos	Description
arm	Arm licensed trademark
●	PIN1 position

Note: The number of characters in each field above is not fixed.

Figure 71 HTQFP Package Marking

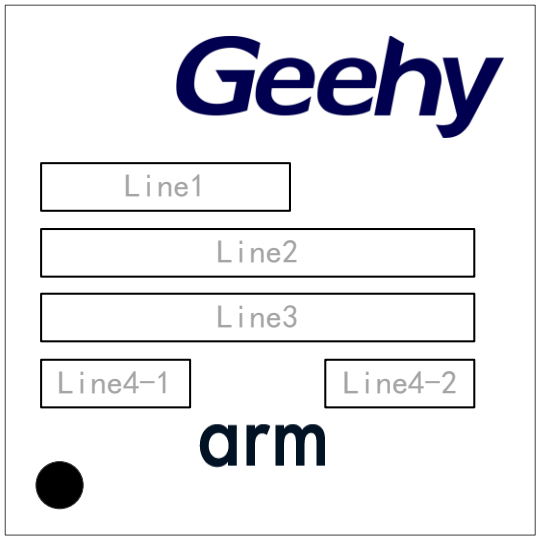


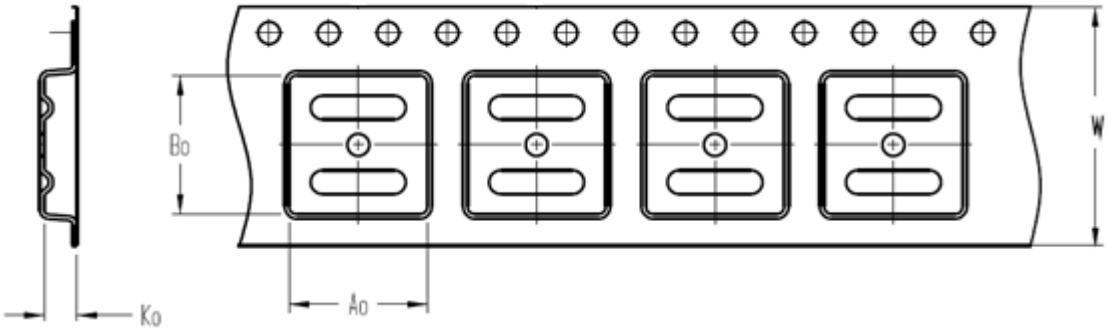
Table 123 Marking Description

Symbols and logos	Description
Geehy	Geehy
Line1	Product series
Line2	Product model
Line3	Product lot number
Line4-1	Internal traceability code
Line4-2	Year and week
arm	Arm licensed trademark
●	PIN1 position

7. Packing Information

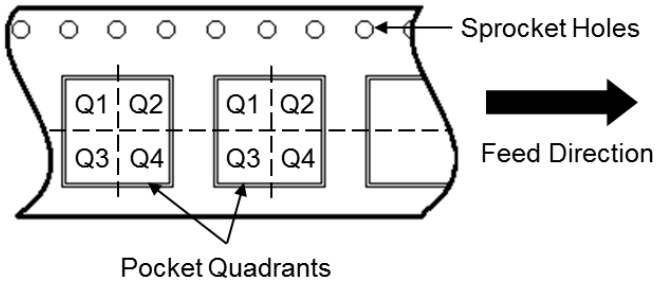
7.1. Tape Packing

Figure 72 Tape Packing Specifications

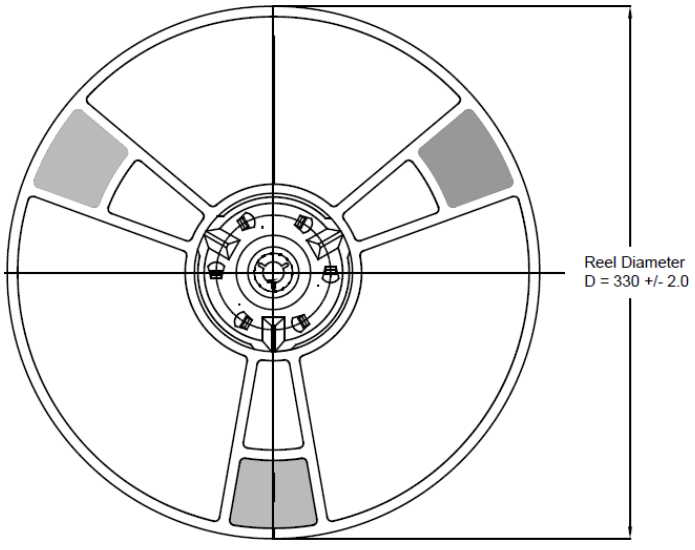


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



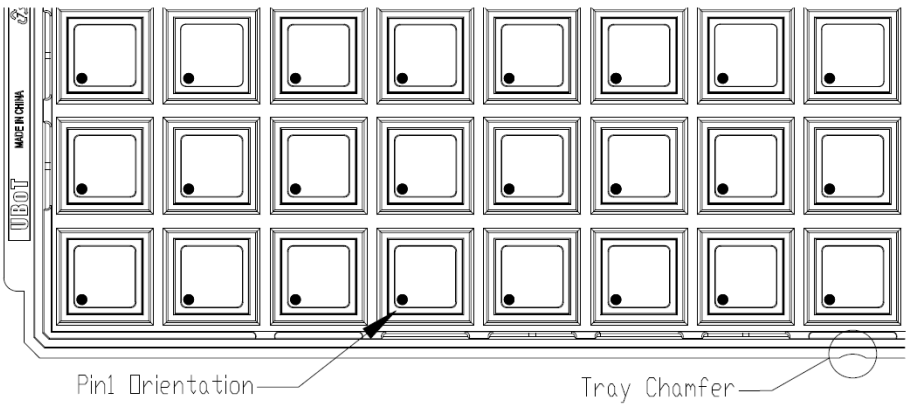
All images are for reference only. Actual product appearance prevails.

Table 124 Tape Packing Specifications

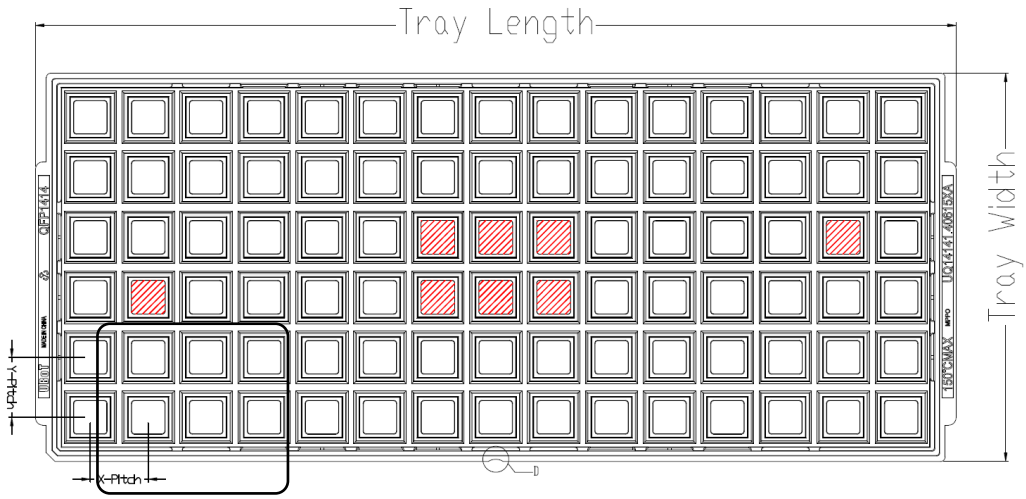
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
G32R502RCT7	LQFP	64	1500	330	12.4	12.4	2.15	24	Q1
G32R502CCE7	HTQFP	48	1000	330	9.4	9.4	1.6	16	Q2
G32R502KCU7	VQFN	32	5000	330	5.3	5.3	0.8	12	Q1
G32R502RCT8	LQFP	64	1500	330	12.4	12.4	2.15	24	Q1
G32R502CCE8	HTQFP	48	1000	330	9.4	9.4	1.6	16	Q2
G32R502KCU8	VQFN	32	5000	330	5.3	5.3	0.8	12	Q1

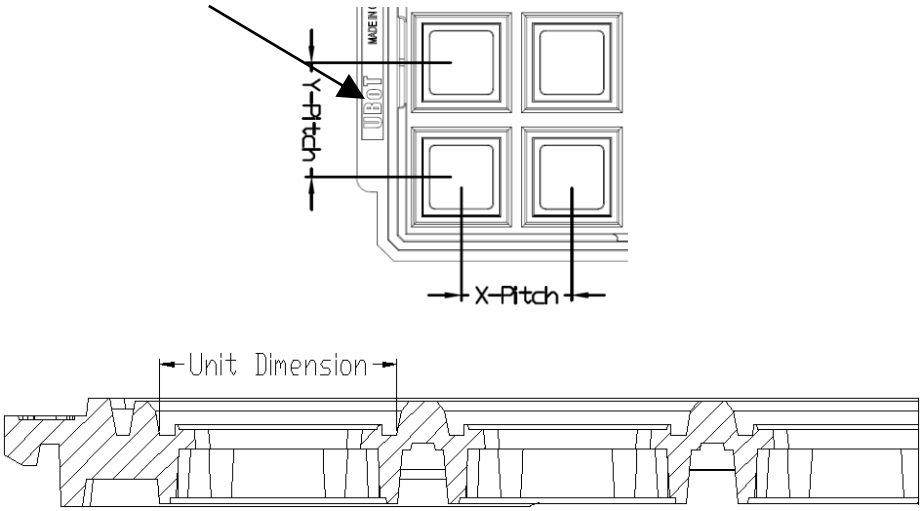
7.2. Tray Packing

Figure 73 Tray Packing Diagram



Tray Dimensions





Note: All images are for reference only. Actual product appearance prevails.

Table 125 Tray Packing Specifications

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
G32R502MCT7	LQFP	80	1190	14.8	14.8	17.9	18	322.6	135.9
G32R502RCT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32R502CCE7	HTQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
G32R502KCU7	VQFN	32	4900	5.2	5.2	8.7	9.0	322.6	135.9
G32R502MCT8	LQFP	80	1190	14.8	14.8	17.9	18	322.6	135.9
G32R502RCT8	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32R502CCE8	HTQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
G32R502KCU8	VQFN	32	4900	5.2	5.2	8.7	9.0	322.6	135.9

8. Ordering Information

Table 126 G32R502 Product Naming Definitions

Product name			
G32R502MCT7			
Naming example	Definition	Naming	Information
G32	Product series	G32	Arm-based 32-bit MCU
R	Product type	R	High-performance real-time controller
5	Core platform	5	Cortex-M52 core
0	Typical features	0	Basic configuration
2	Series number	2	Second product series
M	Pin count	M	80 pins
		R	64 pins
		C	48 pins
		K	32 pins
C	Flash memory capacity	C	256KB
T	Package	T	LQFP
		E	HTQFP
		U	VQFN
7	Temperature range	7	Temperature range: -40℃ to 105℃
		8	Temperature range: -40℃ to 125℃
T	Packing	R	Tape-and-reel packing
		Blank	Tray packing

Table 127 Ordering Information

Ordering code	FLASH(KB)	SRAM(KB)	Package	SPQ	Temperature range
G32R502RCT7-R	256	40	LQFP64	1500	-40℃~105℃
G32R502CCE7-R	256	40	HTQFP48	1000	-40℃~105℃
G32R502KCU7-R	256	40	VQFN32	5000	-40℃~105℃
G32R502RCT8-R	256	40	LQFP64	1500	-40℃~125℃
G32R502CCE8-R	256	40	HTQFP48	1000	-40℃~125℃
G32R502KCU8-R	256	40	VQFN32	5000	-40℃~125℃
G32R502MCT7	256	40	LQFP80	1190	-40℃~105℃
G32R502RCT7	256	40	LQFP64	1600	-40℃~105℃
G32R502CCE7	256	40	HTQFP48	2500	-40℃~105℃
G32R502KCU7	256	40	VQFN32	4900	-40℃~105℃

Ordering code	FLASH(KB)	SRAM(KB)	Package	SPQ	Temperature range
G32R502MCT8	256	40	LQFP80	1190	-40℃~125℃
G32R502RCT8	256	40	LQFP64	1600	-40℃~125℃
G32R502CCE8	256	40	HTQFP48	2500	-40℃~125℃
G32R502KCU8	256	40	VQFN32	4900	-40℃~125℃

9. Common Functional Module Names

Table 128 Common Functional Module Names

Full name	Abbreviation
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCC
External interrupts	EINT
General-purpose I/O	GPIO
Alternate-function I/O	AFIO
Wake-up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power management unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal asynchronous receiver/transmitter	UART
Universal synchronous/asynchronous receiver/transmitter	USART
Flash interface control unit	FMC
Secure digital input/output	SDIO
Digital camera interface	DCI

10. Revision History

Table 129 Document Revision History

Date	Version	Change history
2026.9	1.0	• Initial release

Statement

This document is formulated and published by Geehy Semiconductor Co., Ltd. (hereinafter referred to as “Geehy”). The contents in this document are protected by laws and regulations of trademark, copyright and software copyright. Geehy reserves the right to make corrections and modifications to this document at any time. Read this document carefully before using Geehy products. Once you use the Geehy product, it means that you (hereinafter referred to as the “users”) have known and accepted all the contents of this document. Users shall use the Geehy product in accordance with relevant laws and regulations and the requirements of this document.

1. Ownership

This document can only be used in connection with the corresponding chip products or software products provided by Geehy. Without the prior permission of Geehy, no unit or individual may copy, transcribe, modify, edit or disseminate all or part of the contents of this document for any reason or in any form.

The “极海” or “Geehy” words or graphics with “®” or “™” in this document are trademarks of Geehy. Other product or service names displayed on Geehy products are the property of their respective owners.

2. No Intellectual Property License

Geehy owns all rights, ownership and intellectual property rights involved in this document.

Geehy shall not be deemed to grant the license or right of any intellectual property to users explicitly or implicitly due to the sale or distribution of Geehy products or this document.

If any third party’s products, services or intellectual property are involved in this document, it shall not be deemed that Geehy authorizes users to use the aforesaid third party’s products, services or intellectual property. For any information regarding the application of the product, Geehy hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party, unless otherwise agreed in the sales order or the sales contract.

3. Version Update

Users can obtain the latest document of the corresponding models when ordering Geehy products.

If the contents in this document are inconsistent with Geehy products, the agreement in the sales order or the sales contract shall prevail.

4. Information Reliability

The relevant data in this document are obtained from batch test by Geehy Laboratory or cooperative third-party testing organization. However, clerical errors or errors caused by differences in testing environment may occur inevitably. Therefore, users should understand that Geehy does not bear any responsibility for such errors that may occur in this document. The relevant data in this document are only used to guide users as performance parameter reference and do not constitute Geehy's guarantee for any product performance.

Users shall select appropriate Geehy products according to their own needs, and effectively verify and test the applicability of Geehy products to confirm that Geehy products meet their own needs, corresponding standards, safety or other reliability requirements. If losses are caused to users due to user's failure to fully verify and test Geehy products, Geehy will not bear any responsibility.

5. Legality

USERS SHALL ABIDE BY ALL APPLICABLE LOCAL LAWS AND REGULATIONS WHEN USING THIS DOCUMENT AND THE MATCHING GEEHY PRODUCTS. USERS SHALL UNDERSTAND THAT THE PRODUCTS MAY BE RESTRICTED BY THE EXPORT, RE-EXPORT OR OTHER LAWS OF THE COUNTRIES OF THE PRODUCTS SUPPLIERS, GEEHY, GEEHY DISTRIBUTORS AND USERS. USERS (ON BEHALF OF THEMSELVES, THEIR SUBSIDIARIES AND AFFILIATED ENTERPRISES) SHALL AGREE AND PROMISE TO ABIDE BY ALL APPLICABLE LAWS AND REGULATIONS ON THE EXPORT AND RE-EXPORT OF GEEHY PRODUCTS AND/OR TECHNOLOGIES AND DIRECT PRODUCTS.

6. Disclaimer of Warranty

THIS DOCUMENT IS PROVIDED BY GEEHY "AS IS" AND THERE IS NO WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, TO THE EXTENT PERMITTED BY APPLICABLE LAW.

GEEHY'S PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED FOR USE AS CRITICAL COMPONENTS IN MILITARY, LIFE-SUPPORT, POLLUTION CONTROL, OR HAZARDOUS SUBSTANCES MANAGEMENT SYSTEMS, NOR WHERE FAILURE COULD RESULT IN INJURY, DEATH, PROPERTY OR ENVIRONMENTAL DAMAGE.

IF THE PRODUCT IS NOT LABELED AS "AUTOMOTIVE GRADE," IT SHOULD NOT

BE CONSIDERED SUITABLE FOR AUTOMOTIVE APPLICATIONS. GEEHY ASSUMES NO LIABILITY FOR THE USE BEYOND ITS SPECIFICATIONS OR GUIDELINES.

THE USER SHOULD ENSURE THAT THE APPLICATION OF THE PRODUCTS COMPLIES WITH ALL RELEVANT STANDARDS, INCLUDING BUT NOT LIMITED TO SAFETY, INFORMATION SECURITY, AND ENVIRONMENTAL REQUIREMENTS. THE USER ASSUMES FULL RESPONSIBILITY FOR THE SELECTION AND USE OF GEEHY PRODUCTS. GEEHY WILL BEAR NO RESPONSIBILITY FOR ANY DISPUTES ARISING FROM THE SUBSEQUENT DESIGN OR USE BY USERS.

7. Limitation of Liability

IN NO EVENT, UNLESS REQUIRED BY APPLICABLE LAW OR AGREED TO IN WRITING, WILL GEEHY OR ANY OTHER PARTY WHO PROVIDES THE DOCUMENT AND PRODUCTS "AS IS", BE LIABLE FOR DAMAGES, INCLUDING ANY GENERAL, SPECIAL, DIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OR INABILITY TO USE THE DOCUMENT AND PRODUCTS (INCLUDING BUT NOT LIMITED TO LOSSES OF DATA OR DATA BEING RENDERED INACCURATE OR LOSSES SUSTAINED BY USERS OR THIRD PARTIES). THIS INCLUDES POTENTIAL PERSONAL INJURY, PROPERTY, OR ENVIRONMENTAL DAMAGE, FOR WHICH GEEHY WILL NOT BE RESPONSIBLE.

8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.

9. Language Versions and Artificial Intelligence (AI) Disclaimer

This document is provided in multiple languages, with certain content translated via AI services. In the event of any inconsistency or conflict between the Chinese version and any translated version, the Chinese version shall prevail.

GEEHY ASSUMES NO LIABILITY FOR ANY ERRORS, MISUNDERSTANDINGS, OR MISINTERPRETATIONS ARISING FROM THE USE OF SUCH TRANSLATIONS, OR FROM THE RETRIEVAL, INTERPRETATION, AND PROCESSING OF THIS DOCUMENT'S CONTENT BY THIRD-PARTY AI SYSTEMS.

© 2026 Geehy Semiconductor Co., Ltd. - All Rights Reserved